Product Document

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TSL2580, TSL2581

Light-to-Digital Converter

General Description

The TSL2580 and TSL2581 are very-high sensitivity light-to-digital converters that transform light intensity to a digital signal output capable of direct I^2C (TSL2581) or SMBus (TSL2580) interface. Each device combines one broadband photodiode (visible plus infrared) and one infrared-responding photodiode on a single CMOS integrated circuit capable of providing a near-photopic response over an effective 16-bit dynamic range (16-bit resolution). Two integrating ADCs convert the photodiode currents to a digital output that represents the irradiance measured on each channel. This digital output can be input to a microprocessor where illuminance (ambient light level) in lux is derived using an empirical formula to approximate the human eye response. The TSL2580 device permits an SMB-Alert style interrupt, and the TSL2581 device supports a traditional level style interrupt that remains asserted until the firmware clears it.

While useful for general purpose light sensing applications, the TSL2580/81 devices are designed particularly for display panels (LCD, OLED, etc.) with the purpose of extending battery life and providing optimum viewing in diverse lighting conditions. Display panel backlighting, which can account for up to 30 to 40 percent of total platform power, can be automatically managed. Both devices are also ideal for controlling keyboard illumination based upon ambient lighting conditions. Illuminance information can further be used to manage exposure control in digital cameras. The TSL2580/81 devices are ideal in notebook/tablet PCs, LCD monitors, flat-panel televisions, cell phones, and digital cameras. In addition, other applications include street light control, security lighting, sunlight harvesting, machine vision, and automotive instrumentation clusters.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TSL2580, TSL2581, Light-to-Digital Converter are listed below:

Figure 1:
Added Value Of Using TSL2580, TSL2581

Benefits	Features
• Enables Operation in IR Light Environments	• Patented Dual-Diode Architecture
• Enables Dark Room to High Lux Sunlight Operation	• 1M:1 Dynamic Range
• Digital Interface is Less Susceptible to Noise	• SMBus Digital Interface
• Enables Low Standby Power Consumption	• 3µA Quiescent Current
• Reduces Board Space Requirements while Simplifying Designs	• Available in 1.25mm x 1.75mm Chipscale or 2mm x 2mm Dual Flat No-Lead (FN) Packages

- Approximately 30x More Sensitive Than the TSL2560/61 Device
- Approximates Human Eye Response
- Programmable ALS Interrupt Function with User-Defined Upper and Lower Threshold Settings
- 16-Bit Digital Output with SMBus (TSL2580) at 100 kHz or I^2C (TSL2581) Fast-Mode at 400 kHz
- Programmable Analog Gain and Integration Time Supporting 1,000,000-to-1 Dynamic Range
- Automatically Rejects 50/60-Hz Lighting Ripple

Applications

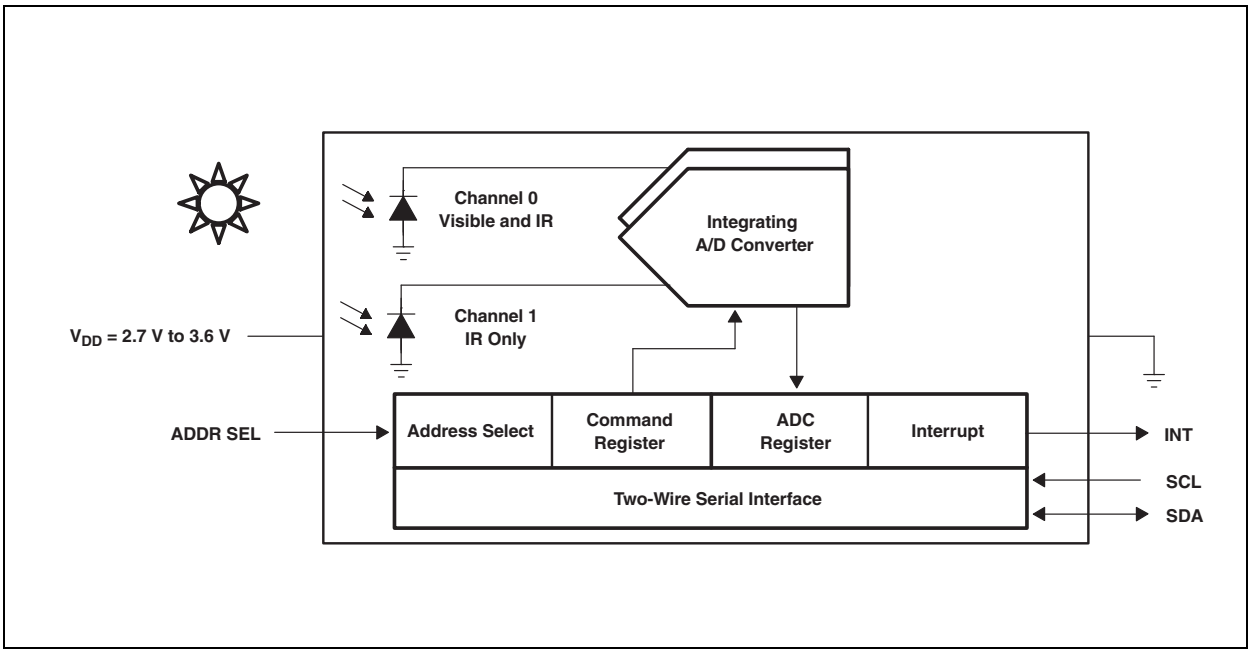
TSL2580, TSL2581, Light-to-Digital Converter is ideal for:

- Ambient Light Sensor (ALS) for Smart Phones, Digital Photo Frames, and Portable Navigation Systems
- ALS for LED Signs, Laptop Computers, and LCD TVs

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TSL2580, TSL2581 Block Diagram



Pin Assignments

The TSL2580, TSL2581 pin assignments are described below:

Figure 3:
Package CS 6-Lead Chipscale

Package CS 6-Lead Chipscale (Top View):
Package Drawings are Not to Scale

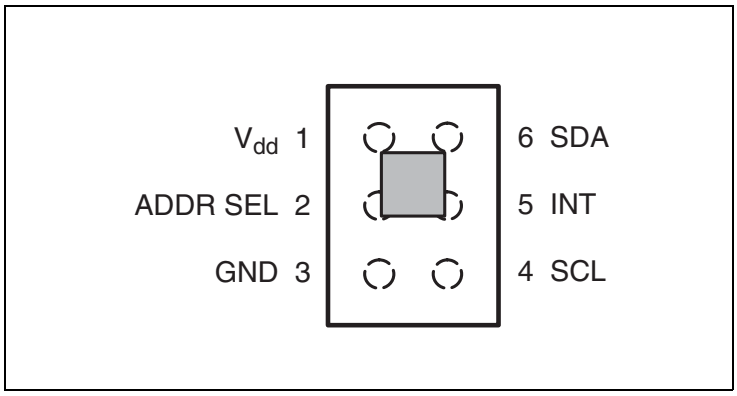


Figure 4:
Package FN Dual Flat No-Lead

Package FN Dual Flat No-Lead (Top View):
Package Drawings are Not to Scale

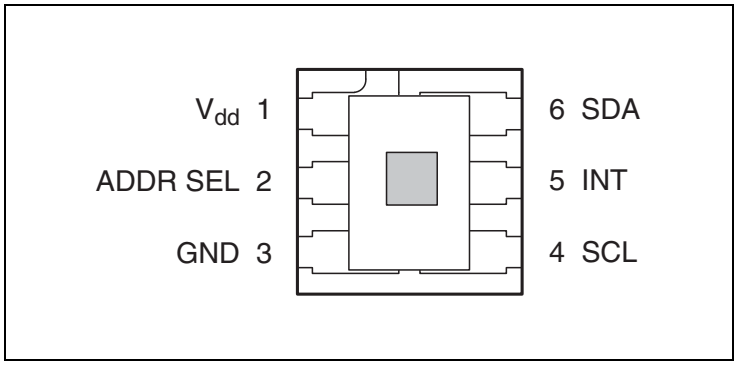


Figure 5:
Terminal Functions

Terminal			Type	Description
Name	CS Pkg No	FN Pkg No		
V_{DD}	1	1		Supply voltage
ADDR SEL	2	2	I	Address select — three-state
GND	3	3		Power supply ground. All voltages are referenced to GND
SCL	4	4	I	Serial clock input terminal — clock signal
INT	5	5	O	Level or SMB Alert interrupt — open drain
SDA	6	6	I/O	Serial data I/O terminal — serial data I/O

Detailed Description

The TSL2580 and TSL2581 are second-generation ambient light sensor devices. Each contains two integrating analog-to-digital converters (ADC) that integrate currents from two photodiodes. Integration of both channels occurs simultaneously. Upon completion of the conversion cycle, the conversion result is transferred to the Channel 0 and Channel 1 data registers, respectively. The transfers are double-buffered to ensure that the integrity of the data is maintained. After the transfer, the device automatically begins the next integration cycle.

Communication to the device is accomplished through a standard, two-wire SMBus or I^2C serial bus. Consequently, the TSL258x device can be easily connected to a microcontroller or embedded controller. No external circuitry is required for signal conditioning, thereby saving PCB real estate as well. Since the output of the TSL258x device is digital, the output is effectively immune to noise when compared to an analog signal.

The TSL258x devices also support an interrupt feature that simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity value. The primary purpose of the interrupt function is to detect a meaningful change in light intensity. The concept of a *meaningful change* can be defined by the user both in terms of light intensity and time, or persistence, of that change in intensity. The TSL258x devices have the ability to define a threshold above and below the current light level. An interrupt is generated when the value of a conversion exceeds either of these limits.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Min	Max	Units
V_{DD} (1)	Supply voltage		3.8	V
V_O	Digital output voltage range	-0.5	3.8	V
I_O	Digital output current	-1	20	mA
T_{strg}	Storage temperature range	-40	85	°C
ESD_{HBM}	ESD tolerance, human body model	±2000		V

Note(s):

1. All voltages are with respect to GND.

Electrical Characteristics

Figure 7:
Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Unit
V_{DD}	Supply voltage		2.7	3	3.6	V
T_A	Operating free-air temperature		-30		70	°C
V_{IL}	SCL, SDA input low voltage	TSL2580(1)			0.8	V
		TSL2581(2)			0.3 V_{DD}	
V_{IH}	SCL, SDA input high voltage	TSL2580(1)	2			V
		TSL2581(2)	0.7 V_{DD}			

Note(s):

1. Meets SMB specifications.
2. Meets I^2C specifications where $V_{DD} = V_{BUS}$.

Figure 8:
Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Active		175	250	µA
		Power down		3	10	µA
V_{OL}	INT, SDA output low voltage	3mA sink current	0		0.4	V
		6mA sink current	0		0.6	V
I_{LEAK}	Leakage current		-5		5	µA

Figure 9:
Operating Characteristics; V_{DD} = 3 V, T_A = 25°C (unless otherwise noted) (1) (2) (3) (4)

Parameter	Test Conditions	Channel	Min	Typ	Max	Unit
Oscillator frequency f_{OSC}			705	750	795	kHz
Dark ADC count value	E_e = 0, ITIME = 0xB6 (200 ms), gain=16x	CH0	0	1	5	counts
		CH1	0	1	5	

Parameter	Test Conditions	Channel	Min	Typ	Max	Unit
Full scale ADC count value	ITIME = 0xDB (100 ms)	CH0			37887	counts
		CH1			37887	
	ITIME = 0x6C (400 ms)	CH0			65535	
		CH1			65535	
ADC count value	λ_p = 625 nm, ITIME = 0xF6 (27 ms), E_e = 171.6 µW/cm^2, gain = 16x	CH0	4000	5000	6000	counts
		CH1		700		
	λ_p = 850 nm, ITIME = 0xF6 (27 ms), E_e = 220 µW/cm^2, gain = 16x	CH0	4000	5000	6000	
		CH1		2750		
ADC count value ratio: CH1/CH0	λ_p = 625 nm		10.8	15.8	20.8	%
	λ_p = 850 nm		41	55	68	
Irradiance responsivity R_e	λ_p = 625 nm, ITIME = 0xF6 (27 ms)	CH0		29.1		counts/ (µW/cm^2)
		CH1		4		
	λ_p = 850 nm, ITIME = 0xF6 (27 ms)	CH0		22.8		
		CH1		12.5		
Gain scaling (relative to 1x)	8x	CH0	7	8	9	x
		CH1	7	8	9	
	16x	CH0	15	16	17	
		CH1	15	16	17	
	111x	CH0	97	107	115	
		CH1	100	115	125	

Note(s):

1. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Visible 640 nm LEDs and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production.
2. The 625 nm irradiance E_e is supplied by an AlInGaP light-emitting diode with the following characteristics: peak wavelength λ_p = 625 nm and spectral halfwidth $\Delta\lambda½$ = 20 nm.
3. The 850 nm irradiance E_e is supplied by a light-emitting diode with the following characteristics: peak wavelength λ_p = 850 nm and spectral halfwidth $\Delta\lambda½$ = 42 nm.
4. The integration time T_{int}, is dependent on internal oscillator frequency (f_{osc}) and on the number of integration cycles (ITIME) in the Timing Register (0xFF) as described in the Register section. For nominal f_{osc} = 750 kHz, nominal T_{int} = 2.7 ms × ITIME.

Figure 10:
AC Electrical Characteristics; V_{DD} = 3 V, T_A = 25°C, (unless otherwise noted)

Symbol	Parameter(1)	Min	Typ	Max	Unit
$t_{(CONV)}$	Conversion time	2.7		688	ms
$f_{(SCL)}$	Clock frequency (I^2C only)	0		400	kHz
	Clock frequency (SMBus only)	10		100	kHz
$t_{(BUF)}$	Bus free time between start and stop condition	1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time	0.6			µs
$t_{(SUSTO)}$	Stop condition setup time	0.6			µs
$t_{(HDDAT)}$	Data hold time	0		0.9	µs
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(LOW)}$	SCL clock low period	1.3			µs
$t_{(HIGH)}$	SCL clock high period	0.6			µs
$t_{(TIMEOUT)}$	Detect clock/data low timeout (SMBus only)	25		35	ms
t_F	Clock/data fall time			300	ns
t_R	Clock/data rise time			300	ns
C_i	Input pin capacitance			10	pF

Note(s):

1. Specified by design and characterization; not production tested.

Parameter Measurement Information

Figure 11:
Timing Diagrams

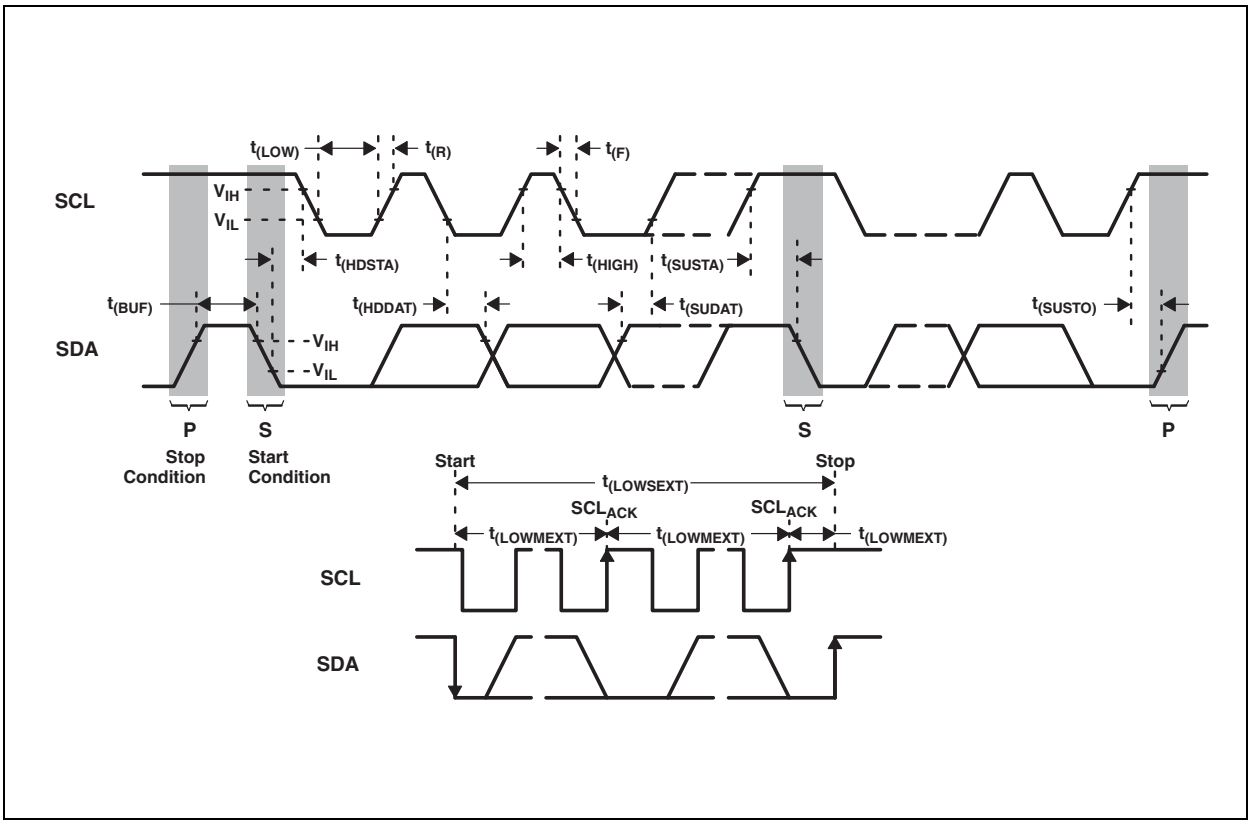


Figure 12:
Example Timing Diagram for SMBus Send Byte Format

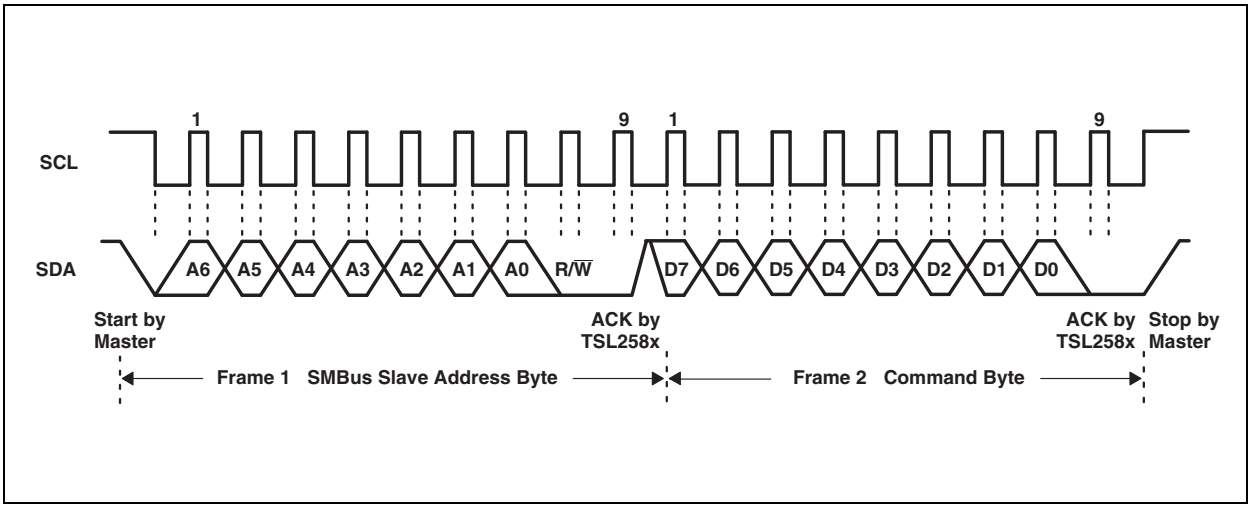
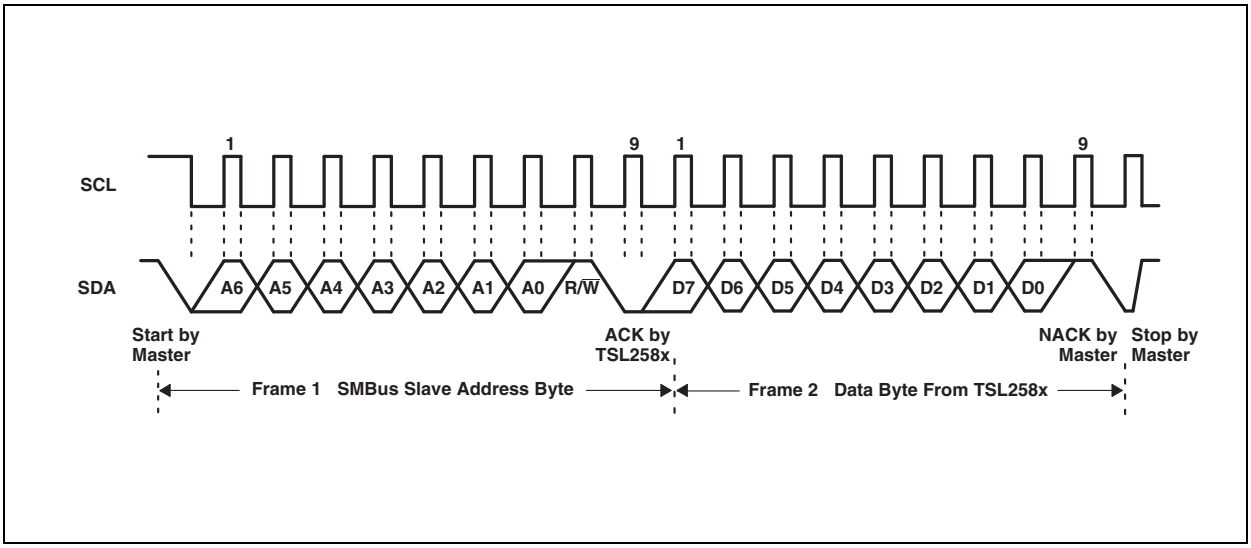


Figure 13:
Example Timing Diagram for SMBus Receive Byte Format



Typical Characteristics

Figure 14:
Spectral Responsivity

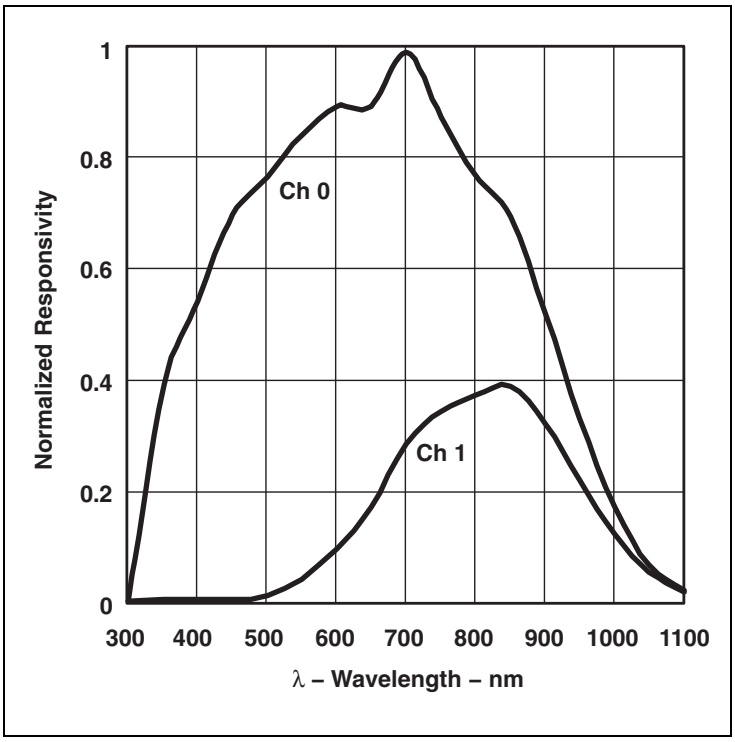
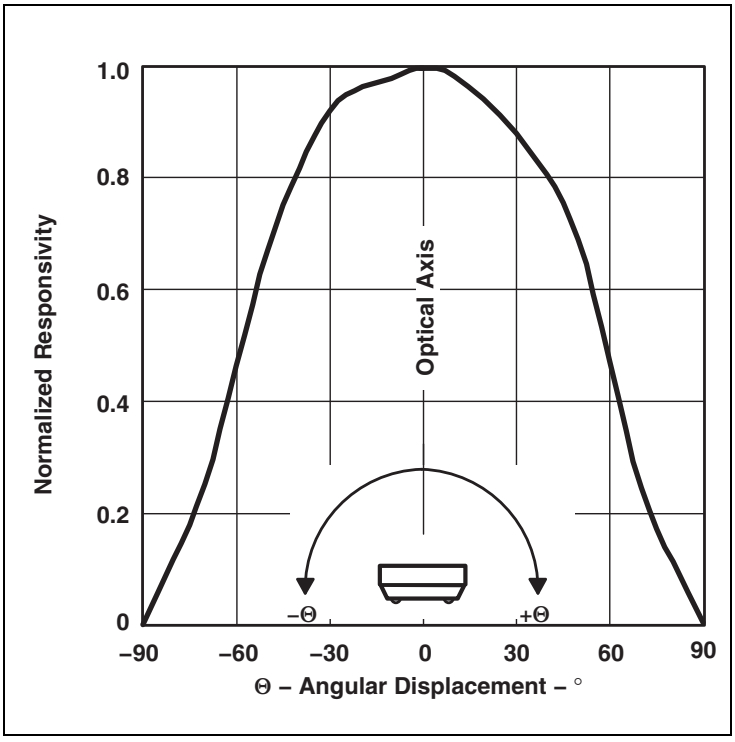


Figure 15:
Normalized Responsivity vs. Angular Displacement



Principles Of Operation

Analog-to-Digital Converter

The TSL258x contains two integrating analog-to-digital converters (ADC) that integrate the currents from the channel 0 and channel 1 photodiodes. Integration of both channels occurs simultaneously, and upon completion of the conversion cycle the conversion result is transferred to the channel 0 and channel 1 data registers, respectively. The transfers are double buffered to ensure that invalid data is not read during the transfer. After the transfer, the device automatically begins the next integration cycle.

Digital Interface

Interface and control of the TSL258x is accomplished through a two-wire serial interface to a set of registers that provide access to device control functions and output data. The serial interface is compatible with System Management Bus (SMBus) versions 1.1 and 2.0, and I^2C bus Fast-Mode. The TSL258x offers three slave addresses that are selectable via an external pin (ADDR SEL). The slave address options are shown in Figure 16.

Figure 16:
Slave Address Selection

Address SEL Terminal Level	Slave Address	SMB Alert Address
GND	0101001	0001100
Float	0111001	0001100
VDD	1001001	0001100

Note(s):

1. The Slave and SMB Alert Addresses are 7 bits. Please note the SMBus and I^2C protocols on pages 10 through 12. A read/write bit should be appended to the slave address by the master device to properly communicate with the TSL258x device.

SMBus and I²C Protocols

Each *Send* and *Write* protocol is, essentially, a series of bytes. A byte sent to the TSL258x with the most significant bit (MSB) equal to 1 will be interpreted as a COMMAND byte. The lower four bits of the COMMAND byte form the register select address (see Figure 26), which is used to select the destination for the subsequent byte(s) received. The TSL258x responds to any Receive Byte requests with the contents of the register specified by the stored register select address.

The TSL2580 implements the following protocols of the SMB 2.0 specification:

- Send Byte Protocol
- Receive Byte Protocol
- Write Byte Protocol
- Write Word Protocol
- Read Word Protocol
- Block Write Protocol
- Block Read Protocol

The TSL2581 implements the following protocols of the Philips Semiconductor I²C specification:

- I²C Write Protocol
- I²C Read (Combined Format) Protocol

When an SMBus Block Write or Block Read is initiated (see description of Command Register), the byte following the COMMAND byte is ignored but is a requirement of the SMBus specification. This field contains the byte count (i.e. the number of bytes to be transferred). The TSL2580 (SMBus) device ignores this field and extracts this information by counting the actual number of bytes transferred before the Stop condition is detected.

When an I²C Write or I²C Read (Combined Format) is initiated, the byte count is also ignored but follows the SMBus protocol specification. Data bytes continue to be transferred from the TSL2581 (I²C) device to Master until a NACK is sent by the Master. The data formats supported by the TSL2580 and TSL2581 devices are:

- Master transmitter transmits to slave receiver (SMBus and I²C):
  - The transfer direction in this case is not changed.
- Master reads slave immediately after the first byte (SMBus only):
  - At the moment of the first acknowledgment (provided by the slave receiver) the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter.
- Combined format (SMBus and I²C):
  - During a change of direction within a transfer, the master repeats both a START condition and the slave address but with the R/W bit reversed. In this case, the master receiver terminates the transfer by generating a NACK on the last byte of the transfer and a STOP condition.

For a complete description of SMBus protocols, please review the SMBus Specification at:

http://www.smbus.org/specs

For a complete description of I²C protocols, please review the I²C Specification at:

www.nxp.com

Figure 17:
SMBus and I²C Packet Protocol Element Key

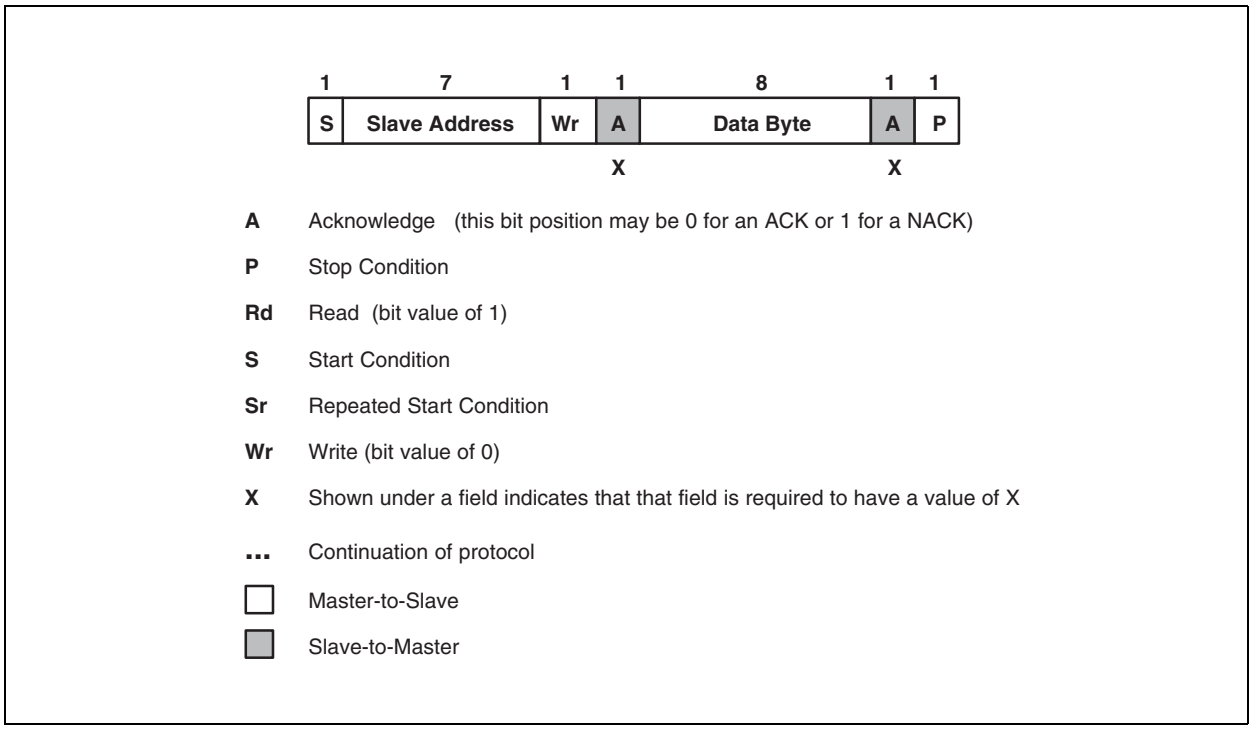


Figure 18:
SMBus Send Byte Protocol

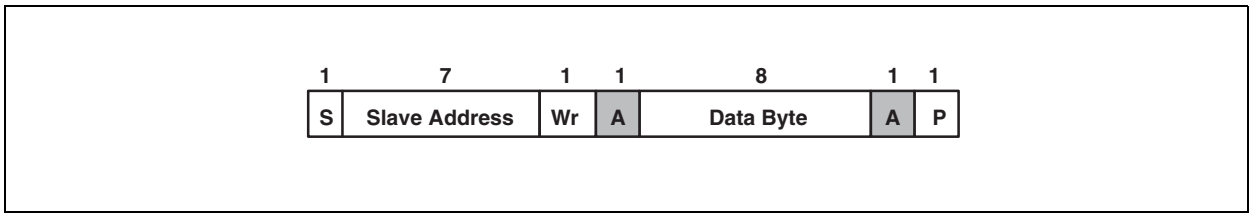


Figure 19:
SMBus Receive Byte Protocol

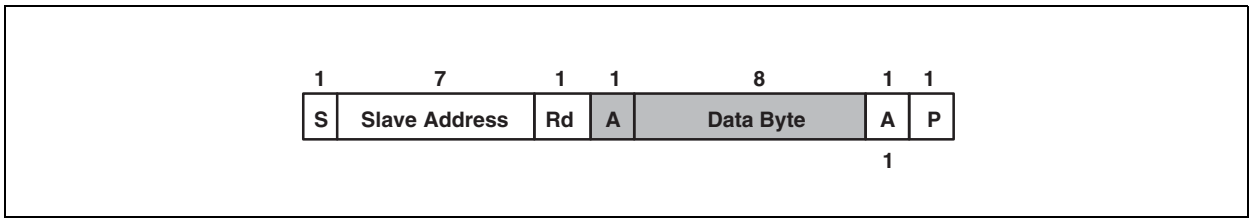


Figure 20:
SMBus Write Byte Protocol

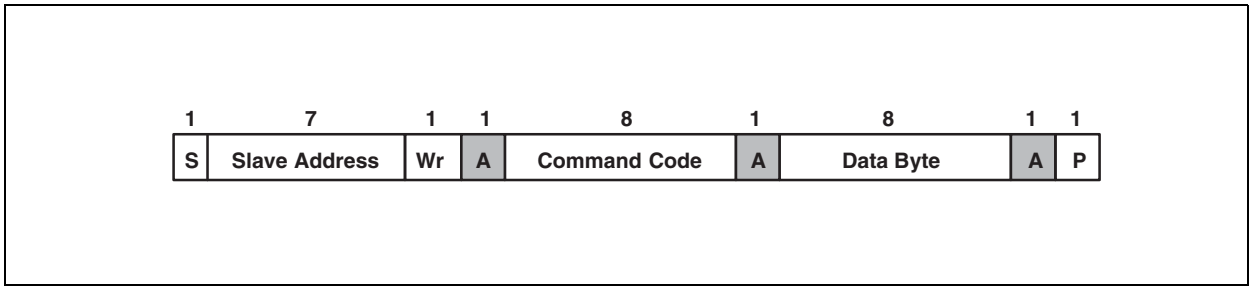


Figure 21:
SMBus Read Byte Protocol

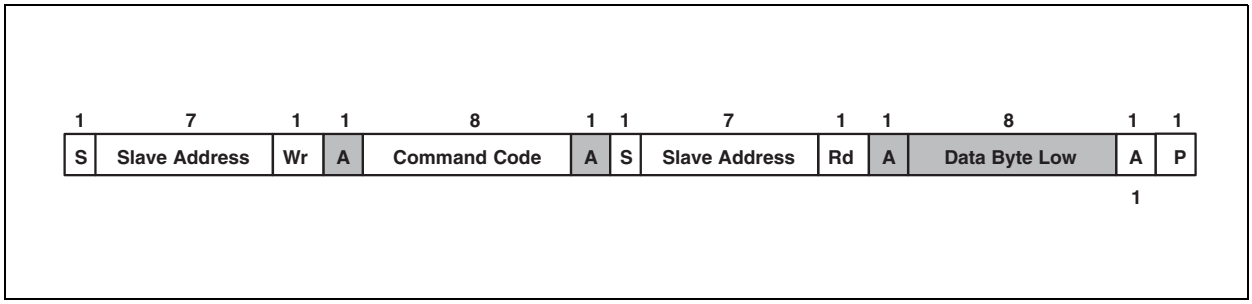


Figure 22:
SMBus Write Word Protocol

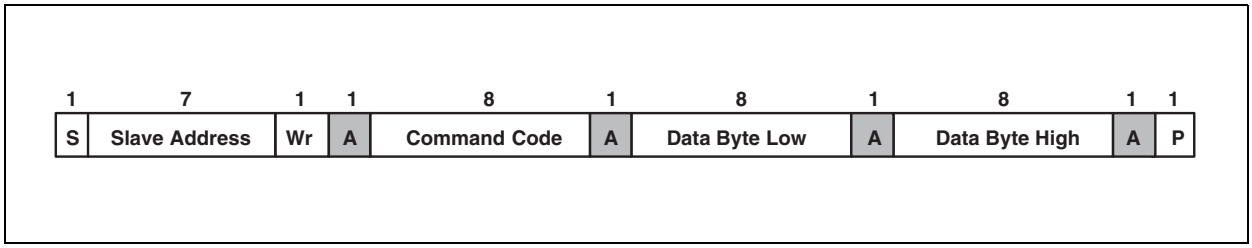


Figure 23:
SMBus Read Word Protocol

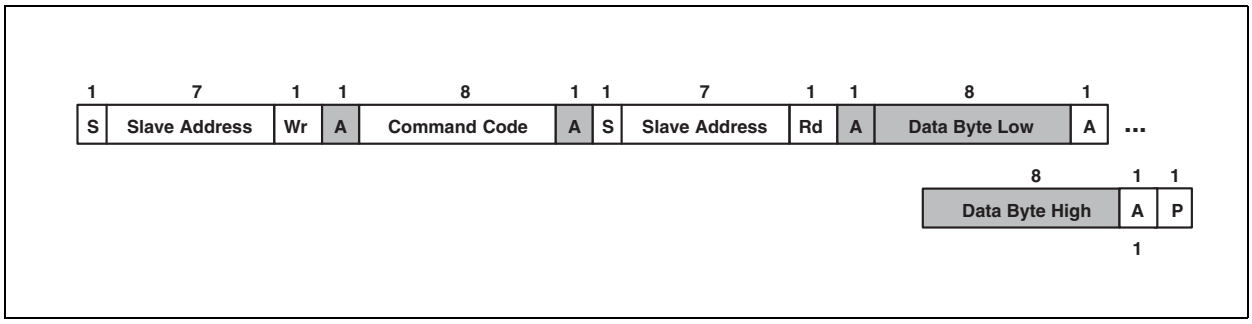
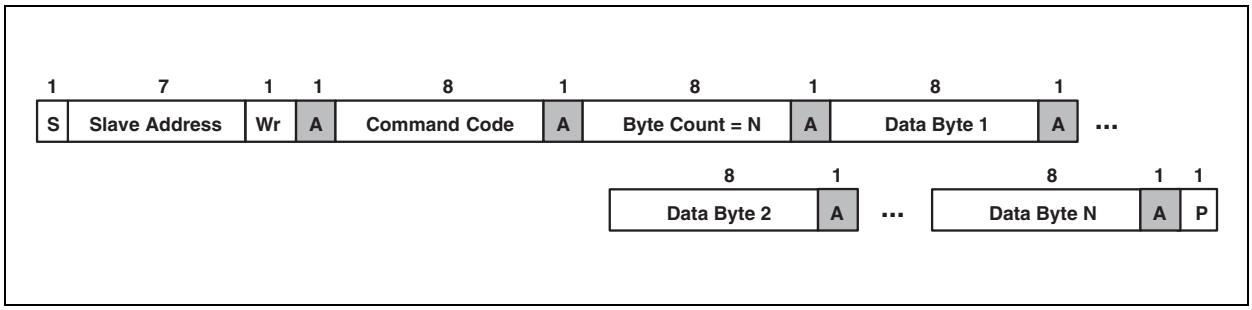


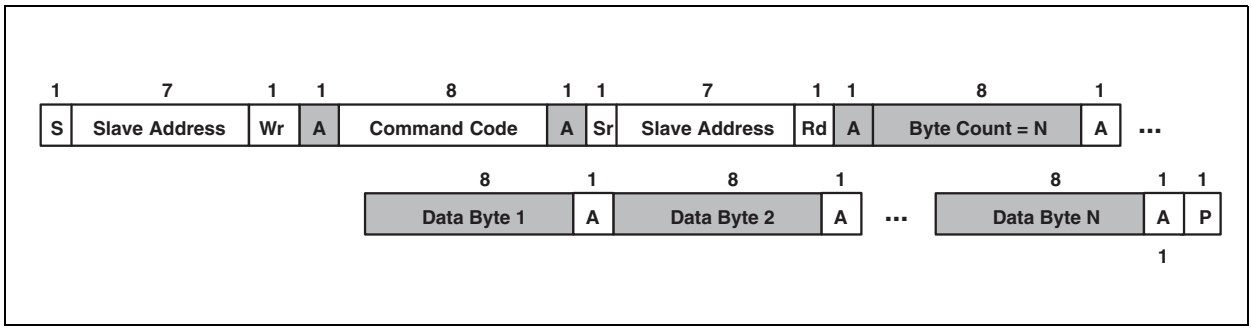
Figure 24:
SMBus Block Write or I²C Write Protocols



Note(s):

1. The I²C write protocol does not use the Byte Count packet, and the Master will continue sending Data Bytes until the Master initiates a Stop condition. See Command Register for additional information regarding the Block Read/Write protocol.

Figure 25:
SMBus Block Read or I²C Read (Combined Format) Protocols



Note(s):

1. The I²C read protocol does not use the Byte Count packet, and the Master will continue receiving Data Bytes until the Master initiates a Stop Condition. See Command Register for additional information regarding the Block Read/Write protocol.

Register Set

The TSL258x is controlled and monitored by sixteen registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Figure 26.

Figure 26:
Register Address

Address	Register Name	Register Function	R/W
––	COMMAND	Specifies register address	W
00h	CONTROL	Control of basic functions	R/W
01h	TIMING	Integration time/gain control	
02h	INTERRUPT	Interrupt control	
03h	THLLOW	Low byte of low interrupt threshold	
04h	THLHIGH	High byte of low interrupt threshold	
05h	THLLOW	Low byte of high interrupt threshold	
06h	THLHIGH	High byte of high interrupt threshold	
07h	ANALOG	Analog control register	
12h	ID	Part number / Rev ID	R
13h	CONSTANT	Number 4 (for SMBus block reads)	
14h	DATA0LOW	ADC channel 0 LOW data register	
15h	DATA0HIGH	ADC channel 0 HIGH data register	
16h	DATA1LOW	ADC channel 1 LOW data register	
17h	DATA1HIGH	ADC channel 1 HIGH data register	
18h	TIMERLOW	Manual integration timer LOW register	
19h	TIMERHIGH	Manual integration timer HIGH register	

The mechanics of accessing a specific register depends on the specific SMB protocol used. See the section on SMBus protocols, above. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

Command Register

The command register specifies the address of the target register for subsequent read and write operations and contains eight bits as described in Figure 27. The command register defaults to 00h at power on.

Figure 27:
Command Register

7	6	5	4	3	2	1	0
CMD	TRANSACTION		ADDRESS				

Field	Bits	Description		
CMD	7	Select Command Register. Must write as 1 when addressing COMMAND register.		
TRANSACTION	6:5	Selects type of transaction to follow in subsequent data transfers:		
		FIELD VALUE	**TRANSACTION**	**DESCRIPTION**
		00	Byte protocol	SMB read/write byte protocol
		01	Word protocol	SMB read/write word protocol
		10	Block protocol	SMB and I^2C read/write block protocol. Regarding SMBus block transfer, see note below.
		11	Special function	Specifies a special command function in the ADDRESS field (see below).

<table>
<tr><th>Field</th><th>Bits</th><th colspan="3">Description</th></tr>
<tr><td rowspan="6">ADDRESS</td><td rowspan="6">4:0</td><td colspan="3">Register Address/Special Function. This field selects the specific control or status register for following write and read commands according to Figure 26. When the TRANSACTION field is set to 11b, this field specifies a special command function as outlined below.</td></tr>
<tr><td>FIELD VALUE</td><td>SPECIAL FUNCTION</td><td>DESCRIPTION</td></tr>
<tr><td>00000</td><td>Reserved</td><td>Reserved. Write as 0000b.</td></tr>
<tr><td>00001</td><td>Interrupt clear</td><td>Clear any pending interrupt and is a write–once–to–clear bit</td></tr>
<tr><td>00010</td><td>Stop manual integration</td><td>When the Timing Register is set to 00h, a SendByte command with the ADDRESS field set to 0010b will stop a manual integration. The actual length of the integration cycle may be read in the MANUAL INTEGRATION TIMER Register.</td></tr>
<tr><td>00011</td><td>Start manual integration</td><td>When the Timing Register is set to 00h, a SendByte command with the ADDRESS field set to 0011b will start a manual integration. The actual length of the integration cycle may be read in the MANUAL INTEGRATION TIMER Register.</td></tr>
<tr><td>x11xx</td><td>Reserved</td><td>Reserved. Write as 11xxb.</td></tr>
</table>

Note(s):

1. An I^2C block transaction will continue until the Master sends a stop condition. See Figure 24 and Figure 25. Unlike the I^2C protocol, the SMBus read/write protocol requires a Byte Count. All four ADC Channel Registers (14h through 17h) can be read simultaneously in a single SMBus transaction. This is the only 32-bit data block supported by the TSL258x SMBus protocol. The TRANSACTION Field Value must be set to 10b, and a read condition should be initiated with a COMMAND CODE of D3h. By using a COMMAND CODE of D3h during an SMBus Block Read Protocol, the TSL258x device will automatically insert the appropriate Byte Count (Byte Count = 4) as illustrated in Figure 25. A write condition should not be used in conjunction with the 13h register.
2. Only the Send Byte Protocol should be used when clearing interrupts.

Control Register (00h)

The CONTROL register primarily used to power the TSL258x device up and down as shown in Figure 28.

Figure 28:
Control Register

7	6	5	4	3	2	1	0
Resv	Resv	ADC_INTR	ADC_VALID	Resv	Resv	ADC_EN	POWER

Field	Bits	Description
Resv	7:6	Reserved. Write as 0.
ADC_INTR	5	ADC Interrupt. Read only. Indicates that the device is asserting an interrupt.
ADC_VALID	4	ADC Valid. Read only. Indicates that the ADC channel has completed an integration cycle.
Resv	3	Reserved. Write as 0.
Resv	2	Reserved. Write as 0.
ADC_EN	1	ADC Enable. This field enables the two ADC channels to begin integration. Writing a 1 activates the ADC channels, and writing a 0 disables the ADCs.
POWER	0	Power On. Writing a 1 powers on the device, and writing a 0 turns it off.

Note(s):

1. ADC_EN and POWER must be asserted before the ADC changes will operate correctly. After POWER is asserted, a 2-ms delay is required before asserting ADC_EN.
2. The TSL258x device registers should be configured before ADC_EN is asserted.

Timing Register (01h)

The TIMING register controls the internal integration time of the ADC channels in 2.7 ms increments. The TIMING register defaults to 00h at power on.

Figure 29:
Timing Register

7	6	5	4	3	2	1	0
ITIME							

Field	Bits	Description
ITIME	7:0	Integration Cycles. Specifies the integration time in 2.7-ms intervals. Time is expressed as a 2's complement number. So, to quickly work out the correct value to write: (1) determine the number of 2.7-ms intervals required, and (2) then take the 2's complement. For example, for a 1 × 2.7-ms interval, 0xFF should be written. For 2 × 2.7-ms intervals, 0xFE should be written. The maximum integration time is 688.5 ms (00000001b). Writing a 0x00 to this register is a special case and indicates manual timing mode. See CONTROL and MANUAL INTEGRATION TIMER Registers for other device options related to manual integration.

INTEG_CYCLES	TIME	VALUE
–	Manual integration	00000000
1	2.7 ms	11111111
2	5.4 ms	11111110
19	51.3 ms	11101101
37	99.9 ms	11011011
74	199.8 ms	10110110
148	399.6 ms	01101100
255	688.5 ms	00000001

Note(s):

1. The Send Byte protocol cannot be used when ITIME is greater than 127 (for example ITIME[7] = 1) since the upper bit is set aside for write transactions in the COMMAND register.

Interrupt Register (02h)

The INTERRUPT register controls the extensive interrupt capabilities of the device. The open-drain interrupt pin is active low and requires a pull-up resistor to VDD in order to pull high in the inactive state. The TSL258x permits both SMB-Alert style interrupts as well as traditional level style interrupts. The Interrupt Register provides control over when a meaningful interrupt will occur. The concept of a meaningful change can be defined by the user both in terms of light intensity and time, or persistence of that change in intensity. The value must cross the threshold (as configured in the Threshold Registers 03h through 06h) and persist for some period of time as outlined in Figure 30.

When a level Interrupt is selected, an interrupt is generated whenever the last conversion results in a value outside of the programmed threshold window. The interrupt is active-low and remains asserted until cleared by writing an 11 in the TRANSACTION field in the COMMAND register.

In SMB-Alert mode, the interrupt is similar to the traditional level style and the interrupt line is asserted low. To clear the interrupt, the host responds to the SMB-Alert by performing a modified Receive Byte operation, in which the Alert Response Address (ARA) is placed in the slave address field, and the TSL258x that generated the interrupt responds by returning its own address in the seven most significant bits of the receive data byte. If more than one device connected on the bus has pulled the SMBAlert line low, the highest priority (lowest address) device will win control of the bus during the slave address transfer. If the device loses this arbitration, the interrupt will not be cleared. The Alert Response Address is 0Ch.

When INTR = 11, the interrupt is generated immediately following the SMBus write operation. Operation then behaves in an SMB-Alert mode, and the software set interrupt may be cleared by an SMB-Alert cycle.

Note(s): Interrupts are based on the value of Channel 0 only.

Figure 30:
Interrupt Control Register

7	6	5	4	3	2	1	0
Resv	INTR_STOP	INTR		PERSIST			

Field	Bits	Description
Resv	7	Reserved. Write as 0.
INTR_STOP	6	Stop ADC integration on interrupt. When high, ADC integration will stop once an interrupt is asserted. To resume operation (1) de-assert ADC_EN using CONTROL register, (2) clear interrupt using COMMAND register, and (3) re-assert ADC_EN using CONTROL register. (1)
INTR	5:4	INTR Control Select. This field determines mode of interrupt logic according to Figure 31, below.
PERSIST	3:0	Interrupt persistence. Controls rate of interrupts to the host processor as shown in Figure 32, below.

Note(s):

1. Use this bit to isolate a particular condition when the sensor is continuously integrating.

Figure 31:
Interrupt Control Select

Intr Field Value	Read Value
00	Interrupt output disabled
01	Level Interrupt
10	SMBAlert compliant
11	Test Mode: Sets interrupt and functions as mode 10

Note(s):

1. Field value of 11 may be used to test interrupt connectivity in a system or to assist in debugging interrupt service routine software.

Figure 32:
Interrupt Persistence Select

Persist Field Value	Interrupt Persist Function
0000	Every ADC cycle generates interrupt
0001	Any value outside of threshold range
0010	2 integration time periods out of range
0011	3 integration time periods out of range
0100	4 integration time periods out of range
0101	5 integration time periods out of range
0110	6 integration time periods out of range
0111	7 integration time periods out of range
1000	8 integration time periods out of range
1001	9 integration time periods out of range
1010	10 integration time periods out of range
1011	11 integration time periods out of range
1100	12 integration time periods out of range
1101	13 integration time periods out of range
1110	14 integration time periods out of range
1111	15 integration time periods out of range

Interrupt Threshold Register (03h - 06h)

The interrupt threshold registers store the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by channel 0 crosses below or is equal to the low threshold specified, an interrupt is asserted on the interrupt pin. If the value generated by channel 0 crosses above the high threshold specified, an interrupt is asserted on the interrupt pin. Registers THLLOW and THLHIGH provide the low byte and high byte, respectively, of the lower interrupt threshold. Registers THHLOW and THHHIGH provide the low and high bytes, respectively, of the upper interrupt threshold. The high and low bytes from each set of registers are combined to form a 16-bit threshold value. The interrupt threshold registers default to 00h on power up.

Figure 33:
Interrupt Threshold Register

Register	Address	Bits	Description
THLLOW	3h	7:0	ADC channel 0 lower byte of the low threshold
THLHIGH	4h	7:0	ADC channel 0 upper byte of the low threshold
THHLOW	5h	7:0	ADC channel 0 lower byte of the high threshold
THHHIGH	6h	7:0	ADC channel 0 upper byte of the high threshold

Note(s):

1. Since two 8-bit values are combined for a single 16-bit value for each of the high and low interrupt thresholds, the Send Byte protocol should not be used to write to these registers. Any values transferred by the Send Byte protocol with the MSB set would be interpreted as the COMMAND field and stored as an address for subsequent read/write operations and not as the interrupt threshold information as desired. The Write Word protocol should be used to write byte-paired registers. For example, the THLLOW and THLHIGH registers (as well as the THHLOW and THHHIGH registers) can be written together to set the 16-bit ADC value in a single transaction.

Analog Register (07h)

The ANALOG register provides eight bits of control to the analog block. These bits control the analog gain settings of the device.

Figure 34:
Analog Register

7	6	5	4	3	2	1	0
RESV						GAIN	

Field	Bits	Description	
Reserved	7:3	Reserved. Write as 0.	
Gain	2:0	Gain Control. Sets the analog gain of the device according to the following table.	
		FIELD VALUE	**GAIN VALUE**
		X00	1x
		X01	8x
		X10	16x
		X11	111x

ID Register (12h)

The ID register provides the value for both the part number and silicon revision number for that part number. It is a read-only register whose value never changes.

Figure 35:
ID Register

7	6	5	4	3	2	1	0
PARTNO				REVNO			

Field	Bits	Description
PARTNO	7:4	Part Number Identification: field value 1000b = TSL2580, field value 1001b = TSL2581
REVNO	3:0	Revision number identification

Constant (13h)

The CONSTANT register provides a means to facilitate SMBus block transfers that is used as the Byte Count in the SMBus protocol. For example, all four ADC Channel Data Registers can be read in a single SMBus block transfer if an SMBus Block Read is initiate at address 13h. This register defaults to the constant 4, but may be set to other values depending upon the end application. For example, if manual integration is employed and the register is set to 5, then all four ADC Channel Data Registers and the Manual Integration Timer Register can be read in a single SMBus read block transaction.

Figure 36:
Constant Register

7	6	5	4	3	2	1	0
CONSTANT							

Field	Bits	Description
CONSTANT	7:0	Constant value used as the byte count for SMBus block read/write transactions. I^2C protocol does not use the byte count field in the block transaction, so this register should be ignored if an TSL2581 device is used.

ADC Channel Data Registers (14h - 17h)

The ADC channel data are expressed as 16-bit values spread across two registers. The ADC channel 0 data registers, DATA0LOW and DATA0HIGH provide the lower and upper bytes, respectively, of the ADC value of channel 0. Registers DATA1LOW and DATA1HIGH provide the lower and upper bytes, respectively, of the ADC value of channel 1. All channel data registers are read-only and default to 00h on power up.

Figure 37:
ADC Channel Data Registers

Register	Address	Bits	Description
DATA0LOW	14h	7:0	ADC channel 0 lower byte
DATA0HIGH	15h	7:0	ADC channel 0 upper byte
DATA1LOW	16h	7:0	ADC channel 1 lower byte
DATA1HIGH	17h	7:0	ADC channel 1 upper byte

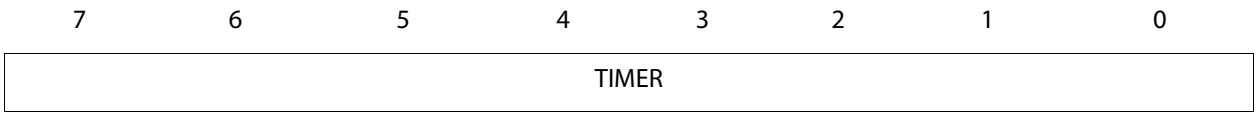
The upper byte data registers can only be read following a read to the corresponding lower byte register. When the lower byte register is read, the upper eight bits are strobed into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Note(s): The Read Word protocol can be used to read byte-paired registers. For example, the DATA0LOW and DATA0HIGH registers (as well as the DATA1LOW and DATA1HIGH registers) may be read together to obtain the 16-bit ADC value in a single transaction

Manual Integration Timer (18h - 19h)

The MANUAL INTEGRATION TIMER registers provide the number of cycles in 10.9 µs increments that occurred during a manual start/stop integration period. The timer is expressed as a 16-bit value across two registers. See Control Register (00h) and Timing Register (01h) for further instructions in configuring a manual integration. The maximum time that can be derived without an overflow is 714.3 ms.

Figure 38:
Manual Integration Timer Registers



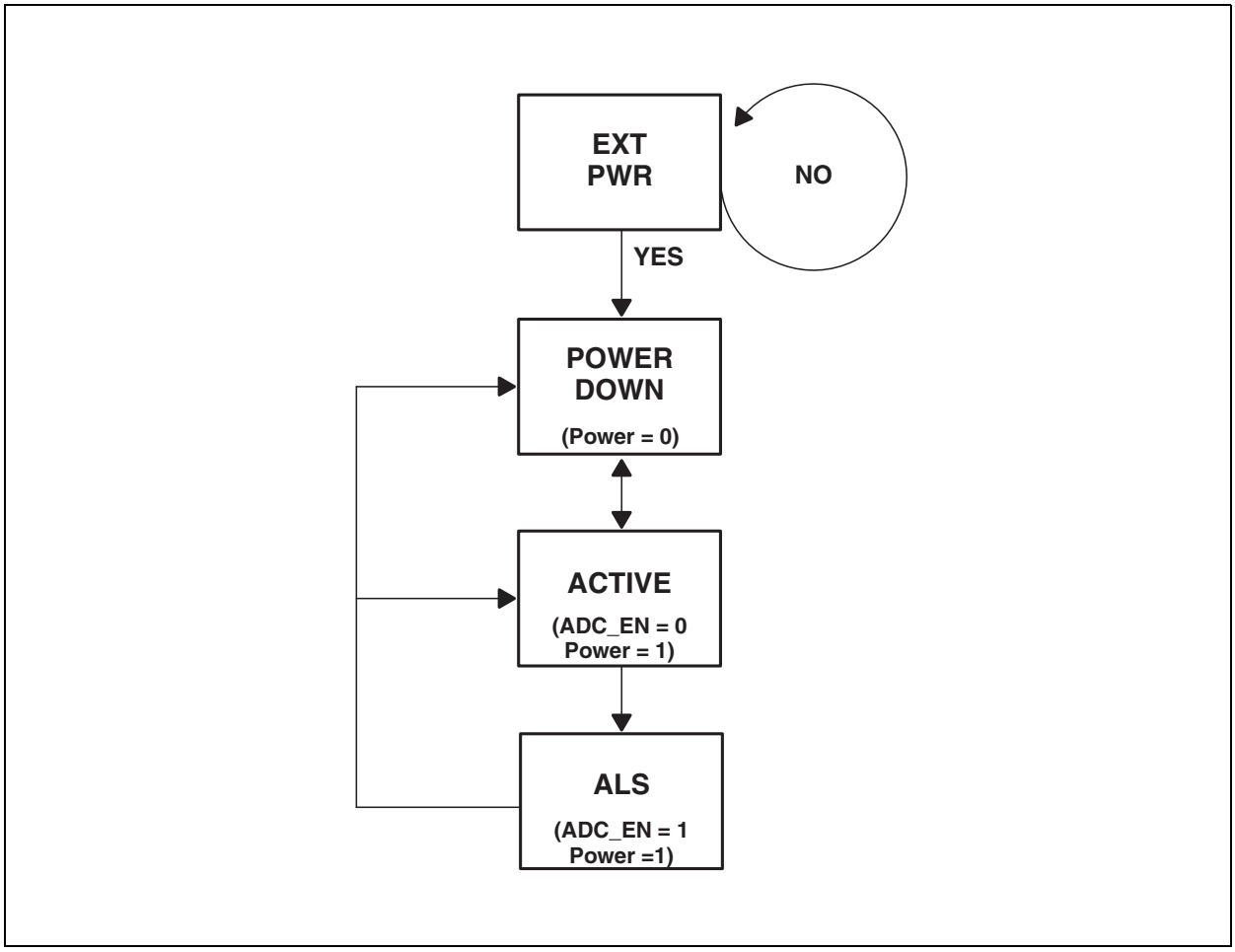
Register	Address	Bits	Description
TIMERLOW	18h	7:0	Manual Integration Timer lower byte
TIMERHIGH	19h	7:0	Manual Integration Timer upper byte

Application Information: Software

Basic Operation

After applying V_{DD}, the device will initially be in the power-down state. To operate the device, issue a command to access the CONTROL register followed by the data value 01h to the CONTROL register to power up the device. The TIMING register should be configured for the preferred integration period, and then the ADC_EN should be set to 1 to enable both ADC channels.

Figure 39:
State Diagram



The following pseudo code illustrates a procedure for reading the TSL258x device (ALS) using word transactions:

```
        Command = 0x80                                  //Set Command bit and Control Reg
        Power_On = 0x01

        //Power on device
        WriteByte (Address, Command, Power_On)

        Command = 0x81                                  //Set Command bit and ALS Timing Reg
        ITIME = 0xb6                                    //200 ms integration cycle

        //Configure ALS Timing Register for 200 ms integration cycle
        WriteByte (Address, Command, ITIME)

        Command = 0x80                                  //Set Command bit and Control Reg
        ADC_En = 0x03                                   //Enable ADC Channels

        //Keep device powered on and enable ADC prior to reading channel data
        WriteByte (Address, Command, ADC_En | Power_On)

// Read ADC Channels Using Read Word Protocol - RECOMMENDED
        //Address the Ch0 lower data register and configure for Read Word
        Command = 0Xb4                                  //Set Command bit and Word bit

        //Reads two bytes from sequential registers 0x14 and 0x15
        //Results are returned in DataLow and DataHigh variables
        ReadWord (Address, Command, DataLow, DataHigh)
        Channel0 = 256 * DataHigh + DataLow

        //Address the Ch1 lower data register and configure for Read Word
        Command = 0xb6                                  //Set Command bit and Word bit

        //Reads two bytes from sequential registers 0x16 and 0x17
        //Results are returned in DataLow and DataHigh variables
        ReadWord (Address, Command, DataLow, DataHigh)
        Channel1 = 256 * DataHigh + DataLow             //Shift DataHigh to upper byte
```

Interrupts

The interrupt feature of the TSL258x device simplifies and improves system efficiency by eliminating the need to poll the sensor for a light intensity value. Interrupt mode is determined by the INTR field in the INTERRUPT CONTROL Register. The interrupt feature may be disabled by writing a field value of 00h to the Interrupt Control Register (02h) so that polling can be performed.

The versatility of the interrupt feature provides many options for interrupt configuration and usage. The primary purpose of the interrupt function is to signal a meaningful change in light intensity. However, it can also be used as an end-of-conversion signal. The concept of a meaningful change can be defined by the user both in terms of light intensity and time, or persistence, of that change in intensity. The TSL258x device implements two

16-bit-wide interrupt threshold registers that allow the user to define thresholds above and below a desired light level. An interrupt will then be generated when the value of a conversion exceeds either of these limits. For simplicity of programming, the threshold comparison is accomplished only with Channel 0. This simplifies calculation of thresholds that are based, for example, on a percent of the current light level. It is adequate to

use only one channel when calculating light intensity differences because, for a given light source, the channel 0 and channel 1 values are linearly proportional to each other and thus both values scale linearly with light intensity.

To further control when an interrupt occurs, the TSL258x device provides an interrupt persistence feature. This feature allows the user to specify a number of conversion cycles for which a light intensity exceeding either interrupt threshold must persist before actually generating an interrupt. This can be used to prevent transient changes in light intensity from generating an unwanted interrupt. With a value of 1, an interrupt occurs immediately whenever either threshold is exceeded. With values of N, where N can range from 2 to 15, N consecutive conversions must result in values outside the interrupt window for an interrupt to be generated. For example, if N is equal to 10 and the integration time is 402 ms, then an interrupt will not be generated unless the light level persists for more than 4 seconds outside the threshold.

Two different interrupt styles are available: Level and SMBus Alert. The difference between these two interrupt styles is how they are cleared. Both result in the interrupt line going active low and remaining low until the interrupt is cleared. A level style interrupt is cleared by selecting the Special Function in the COMMAND register and writing a 0 to the Interrupt Clear field value. The SMBus Alert style interrupt is cleared by an Alert Response as described in the Interrupt Control Register section and SMBus specification.

To configure the interrupt as an end-of-conversion signal so that every ADC integration cycle generates an interrupt, the interrupt PERSIST field in the Interrupt Control Register (02h) is

set to 0000b. Either Level or SMBus Alert style can be used. An interrupt will be generated upon completion of each conversion. The interrupt threshold registers are ignored.

Calculating Lux

The TSL258x is intended for use in ambient light detection applications such as display backlight control, where adjustments are made to display brightness or contrast based on the brightness of the ambient light, as perceived by the human eye. Conventional silicon detectors respond strongly to infrared light, which the human eye does not see. This can lead to significant error when the infrared content of the ambient light is high, such as with incandescent lighting, due to the difference between the silicon detector response and the brightness perceived by the human eye.

This problem is overcome in the TSL258x through the use of two photodiodes. One of the photodiodes (channel 0) is sensitive to both visible and infrared light, while the second photodiode (channel 1) is sensitive primarily to infrared light. An integrating ADC converts the photodiode currents to digital outputs. Channel 1 digital output is used to compensate for the effect of the infrared component of light on the channel 0 digital output. The ADC digital outputs from the two channels are used in a formula to obtain a value that approximates the human eye response in the commonly used Illuminance unit of Lux:

Chipscale Package

For CH1/CH0 = 0.00 to 0.25	Lux = 0.105 CH0 - 0.208 CH1
For CH1/CH0 = 0.25 to 0.38	Lux = 0.1088 CH0 - 0.2231 CH1
For CH1/CH0 = 0.38 to 0.45	Lux = 0.0729 CH0 - 0.1286 CH1
For CH1/CH0 = 0.45 to 0.60	Lux = 0.060 CH0 - 0.10 CH1
For CH1/CH0 > 0.60	Lux/CH0 = 0

ODFN Package

For CH1/CH0 = 0.00 to 0.30	Lux = 0.130 CH0 - 0.240 CH1
For CH1/CH0 = 0.30 to 0.38	Lux = 0.1649 CH0 - 0.3562 CH1
For CH1/CH0 = 0.38 to 0.45	Lux = 0.0974 CH0 - 0.1786 CH1
For CH1/CH0 = 0.45 to 0.54	Lux = 0.062 CH0 - 0.100 CH1
For CH1/CH0 > 0.54	Lux/CH0 = 0

The formulas shown above were obtained by optical testing with fluorescent and incandescent light sources, and apply only to open-air applications. Optical apertures (e.g. light pipes) will affect the incident light on the device.

Simplified Lux Calculation

Below is the argument and return value including source code (shown on following page) for calculating lux with the TSL2581FN. The source code is intended for embedded and/or microcontroller applications. All floating point arithmetic operations have been eliminated since embedded controllers and microcontrollers generally do not support these types of operations. Because floating point has been removed, scaling must be performed prior to calculating illuminance if the integration time is not 400 msec and/or if the gain is not 1x as denoted in the source code on the following pages

```
//*****************************************************************************
//
// Copyright ams AG
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
// Module Name:
// lux.cpp
//
//*****************************************************************************

#define LUX_SCALE 16 // scale by 2^16
#define RATIO_SCALE 9 // scale ratio by 2^9

//--------------------------------------------------
// Integration time scaling factors
//--------------------------------------------------

#define CH_SCALE 16 // scale channel values by 2^16
#define NOM_INTEG_CYCLE 148 // Nominal 400 ms integration. See Timing Register
//--------------------------------------------------
// Gain scaling factors
//--------------------------------------------------
#define CH0GAIN128X 107 // 128X gain scalar for Ch0
#define CH1GAIN128X 115 // 128X gain scalar for Ch1
//--------------------------------------------------
// FN Package coefficients
//--------------------------------------------------
// For Ch1/Ch0=0.00 to 0.30:
        //Lux=0.130*Ch0-0.240*Ch1

// For Ch1/Ch0=0.30 to 0.38:
        // Lux=0.1649*Ch0-0.3562*Ch1
//
// For Ch1/Ch0=0.38 to 0.45:
```

```
        // Lux=0.0974*Ch0-0.1786*Ch1
//
// For Ch1/Ch0=0.45 to 0.54:
        // Lux=0.062*Ch0-0.10*Ch1
//
// For Ch1/Ch0>0.54:
        // Lux/Ch0=0
//
//------------------------------------------------------
#define K1C 0x009A // 0.30 * 2^RATIO_SCALE
#define B1C 0x2148 // 0.130 * 2^LUX_SCALE
#define M1C 0x3d71 // 0.240 * 2^LUX_SCALE

#define K2C 0x00c3 // 0.38 * 2^RATIO_SCALE
#define B2C 0x2a37 // 0.1649 * 2^LUX_SCALE
#define M2C 0x5b30 // 0.3562 * 2^LUX_SCALE

#define K3C 0x00e6 // 0.45 * 2^RATIO_SCALE
#define B3C 0x18ef // 0.0974 * 2^LUX_SCALE
#define M3C 0x2db9 // 0.1786 * 2^LUX_SCALE

#define K4C 0x0114 // 0.54 * 2^RATIO_SCALE
#define B4C 0x0fdf // 0.062 * 2^LUX_SCALE
#define M4C 0x199a // 0.10 * 2^LUX_SCALE

#define K5C 0x0114 // 0.54 * 2^RATIO_SCALE
#define B5C 0x0000 // 0.00000 * 2^LUX_SCALE
#define M5C 0x0000 // 0.00000 * 2^LUX_SCALE
```

```
// lux equation approximation without floating point calculations
////////////////////////////////////////////////////////////////////////////
// Routine: unsigned int CalculateLux(unsigned int ch0, unsigned int ch0, int iType)
//
// Description: Calculate the approximate illuminance (lux) given the raw
// channel values of the TSL2581. The equation if implemented
// as a piece-wise linear approximation.
//
// Arguments: unsigned int iGain - gain, where 0:1X, 1:8X, 2:16X, 3:128X
// unsigned int tIntCycles - INTEG_CYCLES defined in Timing Register
// unsigned int ch0 - raw channel value from channel 0 of TSL2581
// unsigned int ch1 - raw channel value from channel 1 of TSL2581
// unsigned int iType - package type (1:CS)
//
// Return: unsigned int - the approximate illuminance (lux)
//
////////////////////////////////////////////////////////////////////////////
unsigned int CalculateLux(unsigned int iGain, unsigned int tIntCycles, unsigned int ch0,
unsigned int ch1, int iType)
{
        //---------------------------------------------------------------------------
        // first, scale the channel values depending on the gain and integration time
        // 1X, 400ms is nominal setting

        unsigned long chScale0;
        unsigned long chScale1;
        unsigned long channel1;
        unsigned long channel0;

// No scaling if nominal integration (148 cycles or 400 ms) is used
        if (tIntCycles == NOM_INTEG_CYCLE)
            chScale0 = (1 << CH_SCALE);
        else
            chScale0 = (NOM_INTEG_CYCLE << CH_SCALE) / tIntCycles;

        switch (iGain)
        {
            case 0: // 1x gain
                    chScale1 = chScale0;                    // No scale. Nominal setting
                    break;
            case 1: // 8x gain
                    chScale0 = chScale0 >> 3;               // Scale/multiply value by 1/8
                    chScale1 = chScale0;
                    break;
            case 2: // 16x gain
                    chScale0 = chScale0 >> 4;               // Scale/multiply value by 1/16
                    chScale1 = chScale0;
                    break;
            case 3: // 128x gain
                    chScale1 = chScale0 / CH1GAIN128X;      //Ch1 gain correction factor applied
```

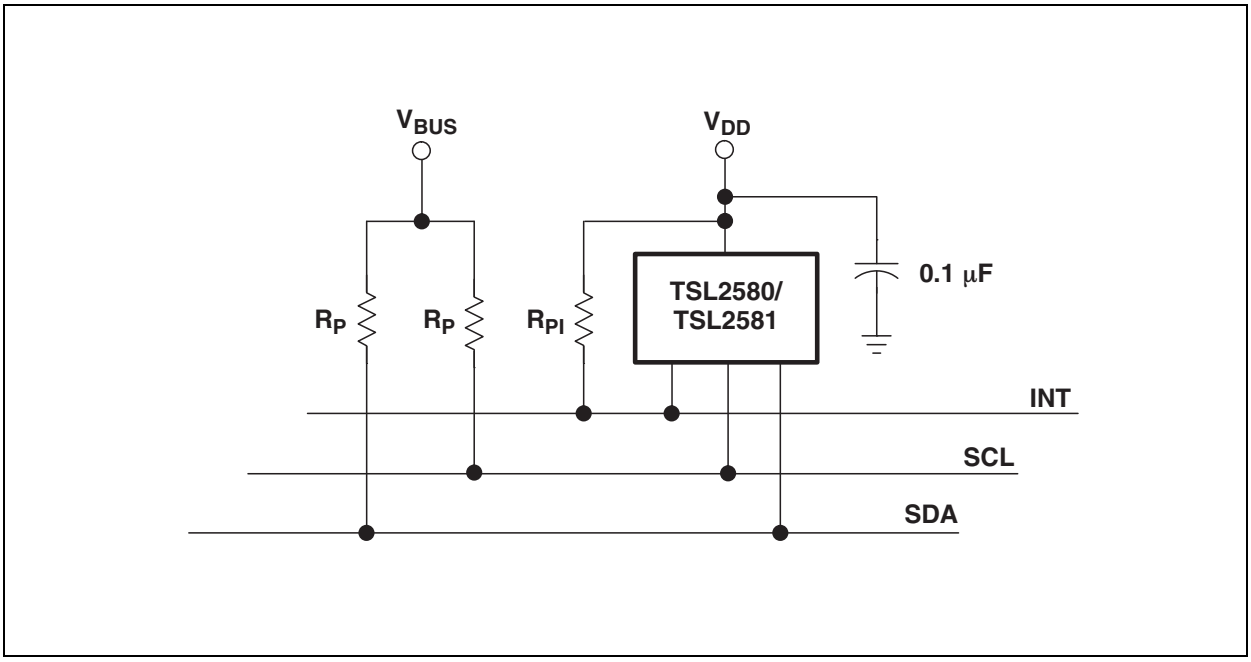
```
                chScale0 = chScale0 / CH0GAIN128X;          //Ch0 gain correction factor applied
                break;
        }
        // scale the channel values
        channel0 = (ch0 * chScale0) >> CH_SCALE;
        channel1 = (ch1 * chScale1) >> CH_SCALE;
        //---------------------------------------------------------------------
        // find the ratio of the channel values (Channel1/Channel0)
        // protect against divide by zero
        unsigned long ratio1 = 0;
        if (channel0 != 0) ratio1 = (channel1 << (RATIO_SCALE+1)) / channel0;
        // round the ratio value
        unsigned long ratio = (ratio1 + 1) >> 1;

        // is ratio <= eachBreak?
        unsigned int b, m;
        switch (iType)
        {
            case 1: // CS package
                if ((ratio >= 0) && (ratio <= K1C))
                    {b=B1C; m=M1C;}
                else if (ratio <= K2C)
                    {b=B2C; m=M2C;}
                else if (ratio <= K3C)
                    {b=B3C; m=M3C;}
                else if (ratio <= K4C)
                    {b=B4C; m=M4C;}
                else if (ratio > K5C)
                    {b=B5C; m=M5C;}
                break;
        }

        unsigned long temp;
        unsigned long lux;
        temp = ((channel0 * b) - (channel1 * m));

        // round lsb (2^(LUX_SCALE-1))
        temp += (1 << (LUX_SCALE-1));
        // strip off fractional portion
        lux = temp >> LUX_SCALE;

        return(lux);
}
```

Application Information: Hardware

Power Supply Decoupling and Application Hardware Circuit

The power supply lines must be decoupled with a 0.1µF capacitor placed as close to the device package as possible (Figure 40). The bypass capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents caused by internal logic switching.

Figure 40:
Bus Pull-Up Resistors



Pull-up resistors (Rp) maintain the SDAH and SCLH lines at a high level when the bus is free and ensure the signals are pulled up from a low to a high level within the required rise time. For a complete description of the SMBus maximum and minimum Rp values, please review the SMBus Specification at:

http://www.smbus.org/specs.

For a complete description of I^2C maximum and minimum Rp values, please review the I^2C Specification at:

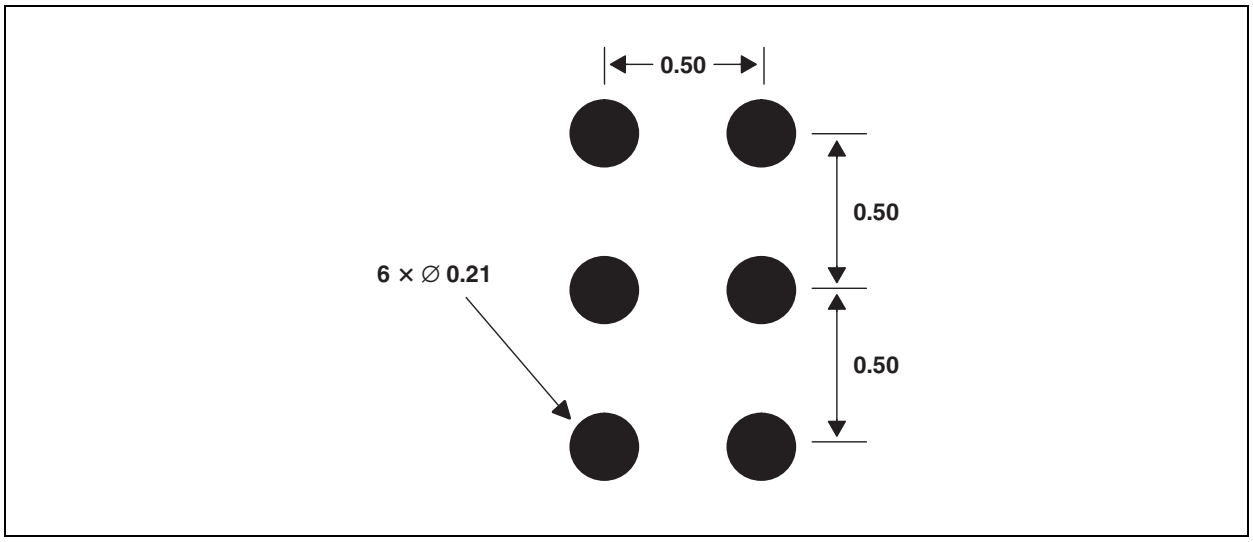
www.nxp.com

A pull-up resistor (R_{PI}) is also required for the interrupt (INT), which functions as a wired-AND signal in a similar fashion to the SCL and SDA lines. A typical impedance value between 10 kΩ and 100 kΩ can be used. Please note that while Figure 40 shows INT being pulled up to V_{DD}, the interrupt can optionally be pulled up to V_{BUS}.

PCB Pad Layouts

Suggested PCB pad layout guidelines for the CS chipscale package are shown in Figure 41.

Figure 41:
Suggested CS Package PCB Layout

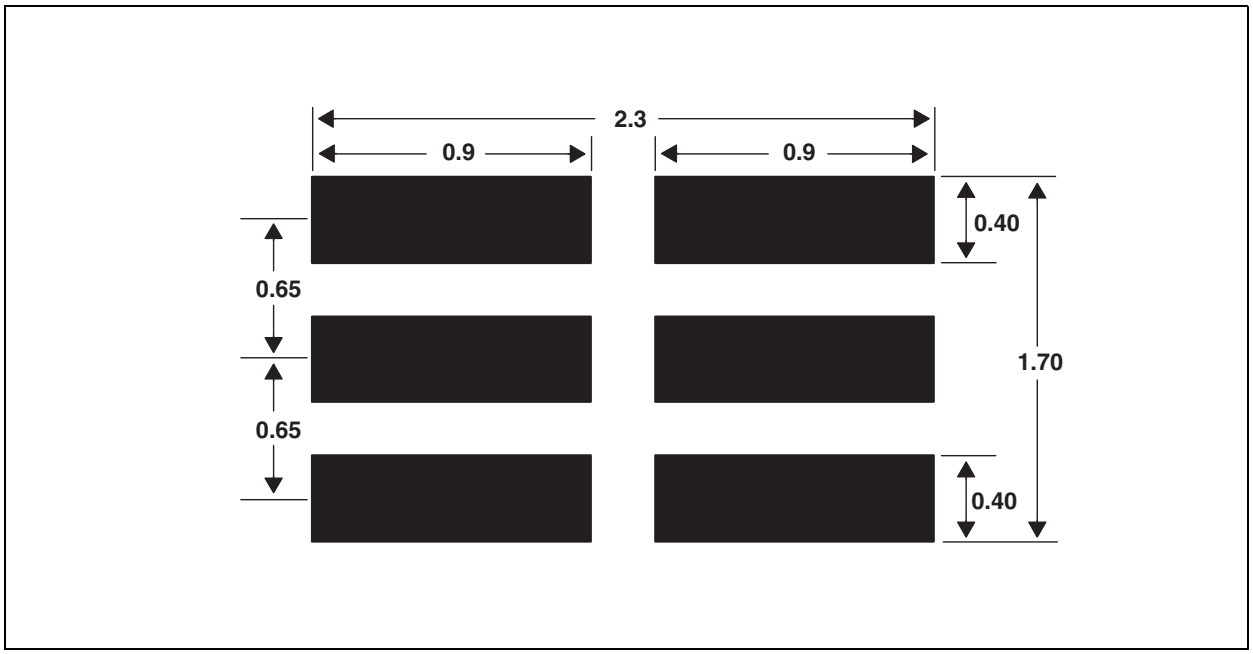


Note(s):

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Suggested PCB pad layout guidelines for the Dual Flat No-Lead (FN) surface mount package are shown in Figure 42.

Figure 42:
Suggested FN Package PCB Layout

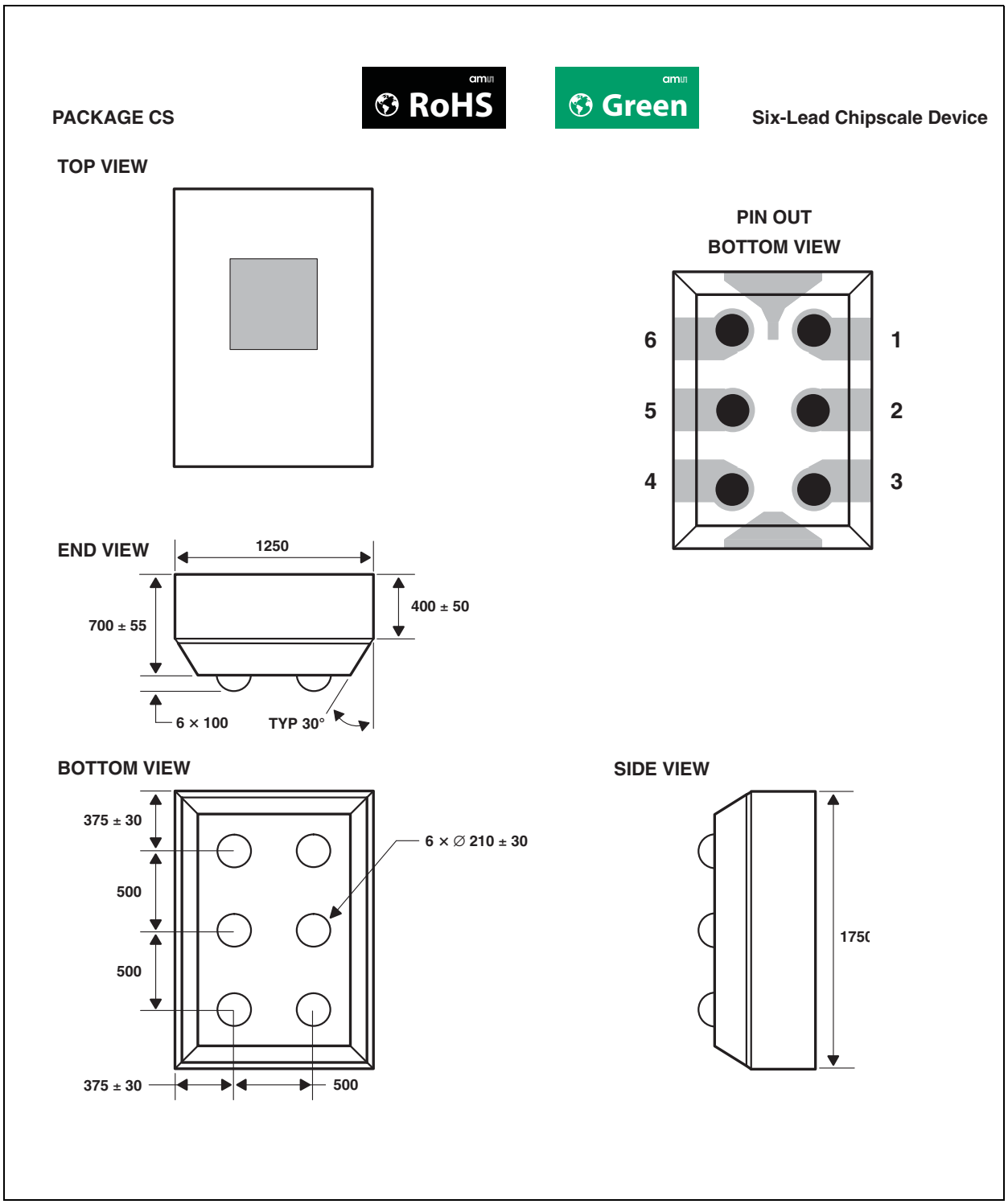


Note(s):

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Mechanical Data

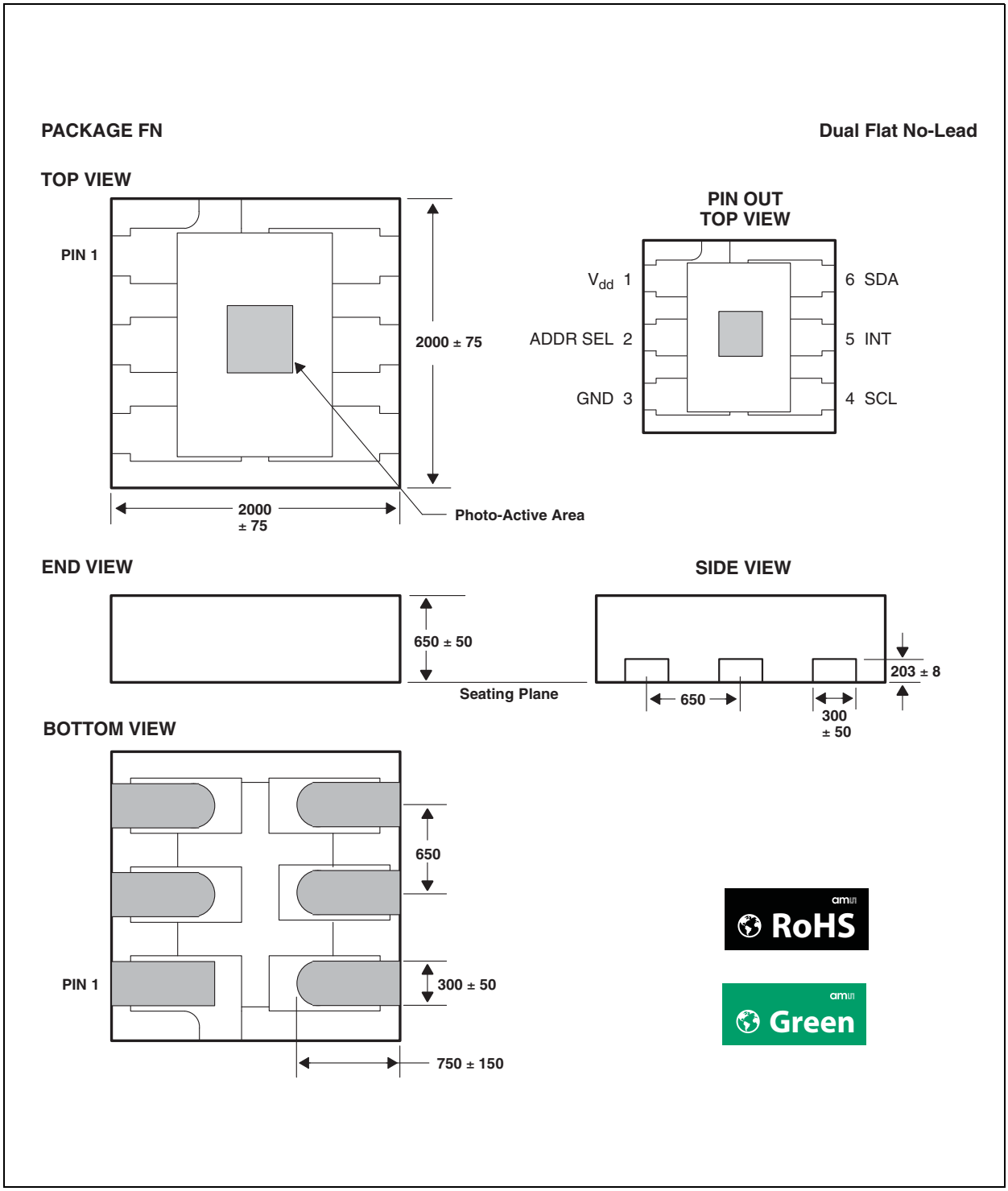
Figure 43:
Package CS — Six-Lead Chipscale Packaging Configuration



Note(s):

1. All linear dimensions are in micrometers. Dimension tolerance is ± 25µm unless otherwise noted.
2. Solder bumps are formed of Sn (96.5%), Ag (3%), and Cu (0.5%).
3. The top of the photodiode active area is 410µm below the top surface of the package.
4. The layer above the photodiode is glass and epoxy with an index of refraction of 1.53.
5. This drawing is subject to change without notice.

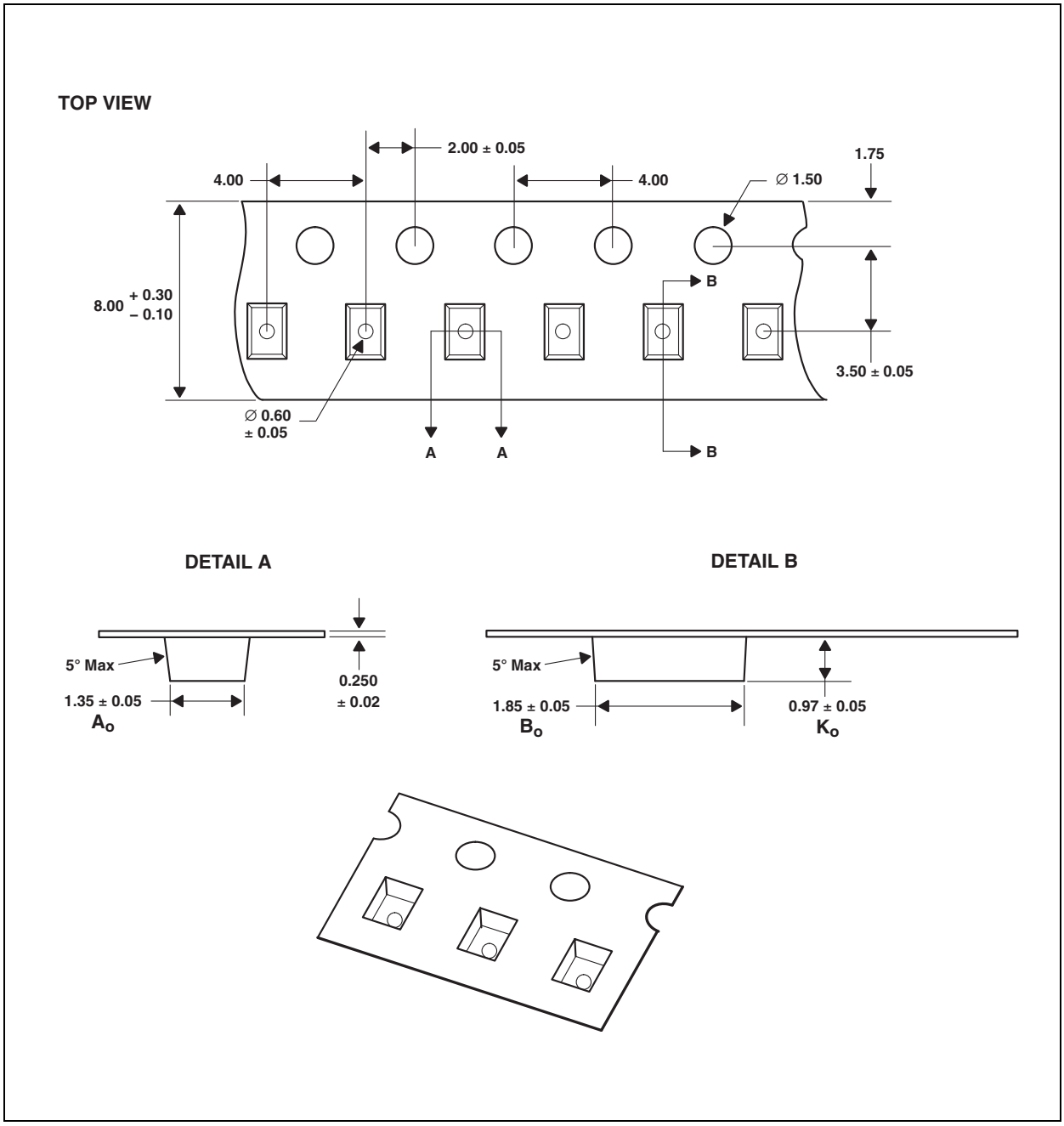
Figure 44:
Package FN — Dual Flat No-Lead Packaging Configuration



Note(s):

1. All linear dimensions are in micrometers. Dimension tolerance is ±20 µm unless otherwise noted.
2. The photodiode active area is 466 µm square and its center is 140 µm above and 20µm to the right of the package center. The die placement tolerance is ± 75 µm in any direction.
3. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
4. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

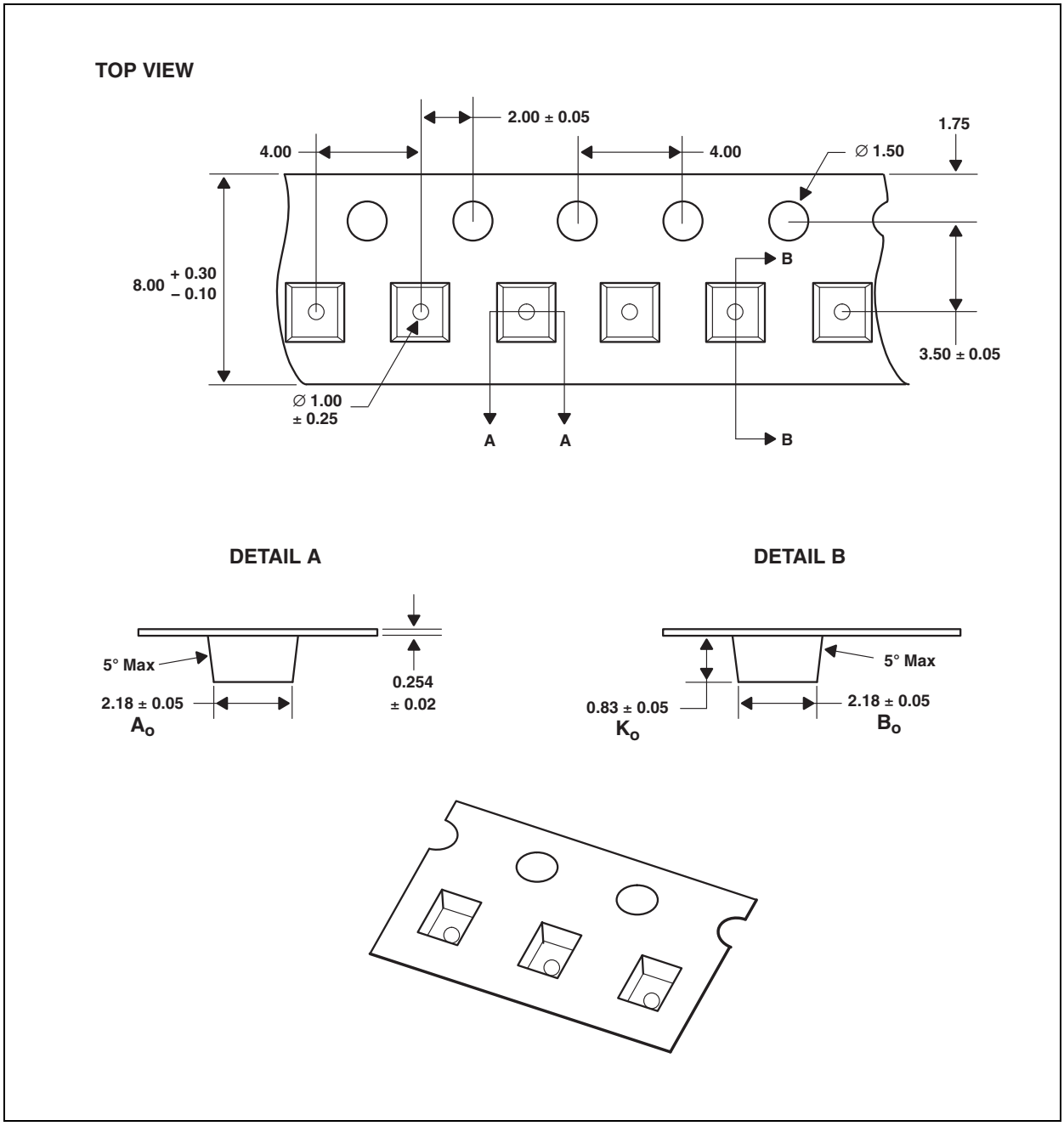
Figure 45:
Package CS Carrier Tape



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ±0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is 178 millimeters in diameter and contains 3500 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481-B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Figure 46:
Package FN Carrier Tape



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ±0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is 178 millimeters in diameter and contains 3500 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481-B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Manufacturing Information

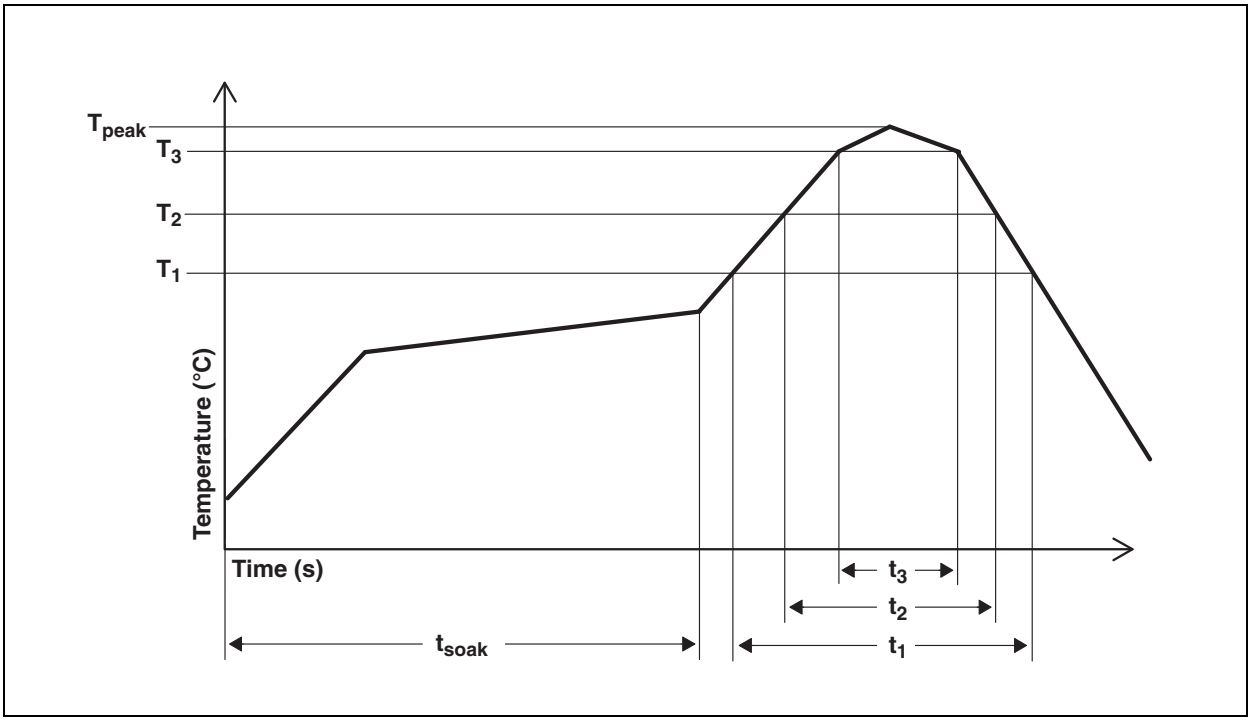
The package has been tested and have demonstrated an ability to be reflow soldered to a PCB substrate. The process, equipment, and materials used in these test are detailed below.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 47:
TSL2580/81 Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5°C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C	t_1	Max 60 s
Time above 230°C	t_2	Max 50 s
Time above T_{peak} –10°C	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260°C (-0°C/+5°C)
Temperature gradient in cooling		Max –5°C/s

Figure 48:
TSL2580/TSL2581 Solder Reflow Profile Graph



Note(s):

1. Not to scale - for reference only.

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package molding compound. To ensure the package molding compound contains the smallest amount of absorbed moisture possible, each device is dry-baked prior to being packed for shipping. Devices are packed in a sealed aluminized envelope with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

CS Package

The CS package has been assigned a moisture sensitivity level of MSL 2 and the devices should be stored under the following conditions:

- Temperature Range: 5°C to 50°C
- Relative Humidity: 60% maximum
- Floor Life: 1 year out of bag at ambient < 30°C / 60% RH

Rebaking will be required if the aluminized envelope has been open for more than 1 year. If rebaking is required, it should be done at 90°C for 3 hours.

FN Package

The FN package has been assigned a moisture sensitivity level of MSL 3 and the devices should be stored under the following conditions:

- Temperature Range: 5°C to 50°C
- Relative Humidity: 60% maximum
- Total Time: 6 months from the date code on the aluminized envelope — if unopened
- Opened Time: 168 hours or fewer

Rebaking will be required if the devices have been stored unopened for more than 6 months or if the aluminized envelope has been open for more than 168 hours. If rebaking is required, it should be done at 90°C for 4 hours.

Ordering & Contact Information

Figure 49:
Ordering Information

Ordering Code	Device	Interface	Package - Leads	Package Designator
TSL2580CS	TSL2580	SMBus	Chipscale–6	CS
TSL2580FN	TSL2580	SMBus	Dual Flat No-Lead–6	FN
TSL2581FN	TSL2581	I^2C	Dual Flat No-Lead–6	FN

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 098 (2010-Mar) to current revision 1-00 (2016-Apr-05)	Page
Content of TAOS datasheet was updated to latest **ams** design	
Updated Key Benefits & Features	2

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision
2. Correction of typographical errors is not explicitly mentioned.

Content Guide