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AS3688

Flexible Lighting Management Unit (Charge Pump, DCDC Step Up, Current Sink, ADC, LDO)

1 General Description

The AS3688 is a highly-integrated CMOS Power and Lighting Management Unit to supply power to LCD-and cameramodules in mobile telephones, and other 1-cell Li+ or 3-cell NiMH powered devices.
The AS3688 incorporates one low-power, low-dropout regulator (LDO), one Step Up DC/DC Converter for white backlight LEDs, one high-power Charge Pump for camera flash LEDs, one Analog-to-Digital Converter, support for up to 11 current sinks, a two wire serial interface, and control logic all onto a single device. Fully programmable.
The AS3688 is a successor to the austrimicrosystems AS3681 with several additional features (Charge Pump Automatic Up Switching, Extended timer features, autonomous logarithmic PWM dimming, LED pattern generator, DCDC step up overvoltage protection, improved Charge Pump and a fourth high current sink).

2 Key Features

New features of the AS3688 compared to the AS3681 are written in ***boldface italics***.

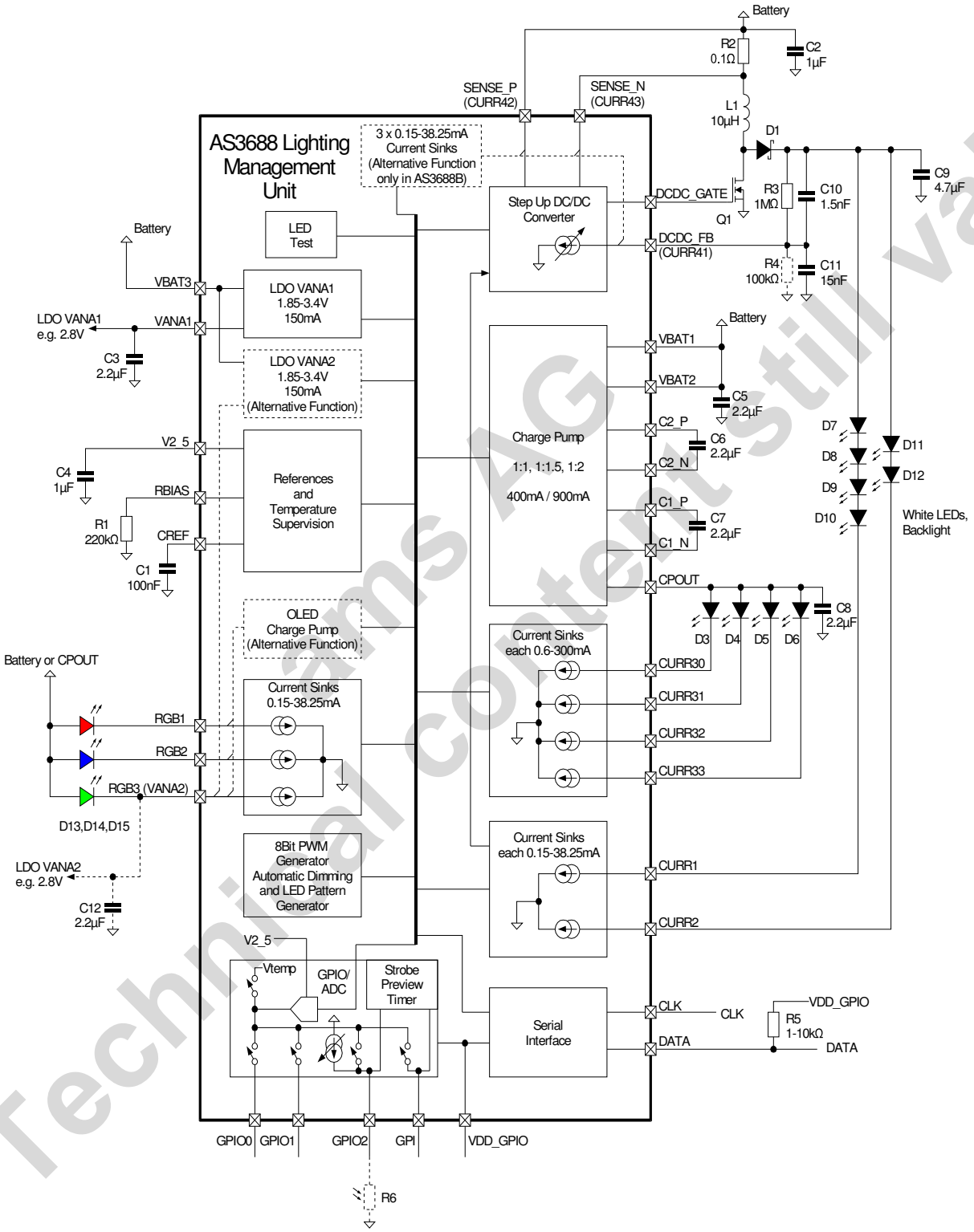
- Programmable High-Performance Regulator
  - Low-Noise LDO (1.85 to 3.4V, 150mA)
  - ***Default off*** after Power-up
  - 3µA Quiescent Current in Standby
  - Programmable via Serial Interface
- High-Efficiency Step Up DC/DC Converter
  - Up to 25V/50mA for White LEDs
  - Programmable Output Voltage with External Resistors and Serial Interface
  - ***Overvoltage Protection***
  - ***0.1Ohm*** Shunt Resistor
- High-Efficiency High-Power Charge Pump
  - 1:1, 1:1.5, and 1:2 Mode
  - ***Automatic Up Switching (can be disabled and 1:2 mode can be blocked)***
  - Output Current up to 400mA / ***900mA pulsed***
  - Efficiency up to 95%
  - ***Very Low effective Resistance*** (0.5Ω typ. 1Ω max. in 1:1 mode, ***1.4Ω typ. 2Ω max***. in 1:1.5)
  - Only 4 External Capacitors Required: 2 x 1µF Flying Capacitors, 2 x 2.2µF
  - Supports LCD White Backlight LEDs,
  - Camera Flash White LEDs, and Keypad Backlight LEDs
- Supports up to ***12*** Current Sinks
  - ***Four*** Programmable (***8+1Bit***) from: ***0.6mA to 300mA***
  - Two High Voltage Programmable (***8-bit***) from: ***0.15mA to 38.25mA***
  - Three Programmable (***8-bit***) from: ***0.15mA to 38.25mA*** for RGB LEDs
  - Three (AS3688B only; AS3688: One) Programmable (***8-bit***) from: ***0.15mA to 38.25mA*** for General Purpose
  - Programmable Hardware Control (Strobe, ***and Preview*** or PWM)
  - Selectively Enable/Disable Current Sinks
- ***Internal PWM Generation***
  - 8 Bit resolution
  - Logarithmic up/down dimming
- ***Led Pattern Generator***
  - ***Autonomous driving for any LED***
- 10-bit Successive Approximation ADC
  - 27µs Conversion Time
  - ***Four*** Selectable Inputs: GPIO0-3
  - ***Internal Temp. Measurement***
  - ***Support for Light Sensor, inluding a adjustable current source (0-15uA)***
- **Support for automatic LED function testing (open and shorted LEDs can be identified)**
- ***Support for external Temperature Sensor for high current LED protection (CURR3x)***
- Strobe Timeout protection
  - ***Up to 1600ms***
  - ***Three different timing modes***
- ***TXMask function (reduce current during Strobe) selectable on pin GPIO1***
- Four General Purpose Inputs/Outputs
  - GPIO0-2 Input/Output, ***GPI only Input***
  - Digital Input, Digital Output, and Tristate
  - Programmable Pull-Up, and Pull-Down
  - ***GPI*** can be used as Flash Strobe
  - ***GPIO2 can be used for Preview Mode***
  - ***GPIO0/2 can used for PWM input***
- Negative or High-Voltage Charge Pump
  - Regulated Output Voltage, Programmable by Dual Resistors e.g. -6V, 10mA for OLED or ±15V, 5mA for TFT
  - ±5% Accuracy
- Standby LDO always on
  - Regulated 2.5V max. output 10mA
  - 3µA Quiescent Current
- Wide Battery Supply Range: 3.0 to 5.5V
- Two Wire Serial Interface Control
- Overcurrent and Thermal Protection
- Package ***QFN32 5x5mm***

3 Application

Power- and lighting-management for mobile telephones and other 1-cell Li+ or 3-cell NiMH powered devices.

4 Block Diagram

Figure 1 – Application Diagram of the AS3688: Option shown: Step up DCDC converter, RGB Current Sinks



Revision History

Revision	Date	Owner	Description
1.0	30.3.2006	tje,ptr	- Fixed typo for vtuning range - Corrected full scale value for current sinks from 38.5mA to 38.25mA (blockdiagram and one overview) - Typical CP power consumption updated - Reduced CP effective resistance in 1:2 mode, efficiency, Vcpout updated, quiescent current consumption - Efficiency diagram of CP added - Changed charge pump output capacitor to 1.5uF minimum - Changed default state for curr_3x_on_cp to 0 - Updated ASIC ID1 and ID2 register position - Updated LED Testing procedure - Updated Mode Switching Diagram (and->or) - Register Map Table updated - slow LED pattern (bit pattern_slow added) - GPIO2 current source modified - polarity control of external overtemp comparator added - Increased standby current consumption by 2uA - Added comment to avoid current source on and 0mA setting - Added comment for preview_off_after strobe - Removed cp_start_debounce - Added comment not to use softdim_pattern for CURR1,CURR2 and CURR3x mode 'Other' - Added comment for order of setting of pattern_data - Changed to 'Datasheet' from 'Preliminary Datasheet'
1.1	23.6.2006	tje,ptr	- Update Application Diagram - Included AS3688B version (for CURR42, CURR43) - Improved Current Sink Matching to 8%; added comment for current sink voltage compliance for accuracy spec - Updated minimum value C6,C7 - Updated Vrsense* (DCDC step up) - Replaced 'FuseReg*' by their actual default value - TTOL +/-5° move from min/max to typical value and removed comment 'Design Target' - Added comment about ADC Reference (V2_5) - Improved voltage compliance of RGB current sinks to V(CPOUT) - Removed CSP Version (use austriamicrosystems AS3689) - Added ADC Temperature measurement coefficients - Removed fuse I2C_Add (replace by comment about factory programmability) - Added comment in LED test for reduced settling time for the DCDC step up converter - Added DCDC efficiency curve - Added ICP1_1.5 and ICP1_2 max. - Added VPGIO rising max; and comment for V_{POR_VBAT} - Added comment for LDO startup
1.1.1	7.7.2006	tje,ptr	- Added maximum value for I_{ACTIVE} - Added maximum value for I_{LIMIT} - Reduced $I_{CP1\_1.5}$

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5 Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 5 Electrical Characteristics is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1 – Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{IN_HV}	15V Pins	-0.3	17	V	Applicable for high-voltage current sink pins $CURR_1$ and $CURR_2$.
V_{IN_MV}	5V Pins	-0.3	7.0	V	Applicable for 5V pins V_{BAT1}:V_{BAT3}, V_{ANA1}, $CURR_{30}$:$CURR_{33}$; C_{1_N}, C_{2_N}, C_{1_P}, C_{2_P}, CPOUT; SENSE_N, SENSE_P, DCDC_FB, DCDC_GATE; $CURR_{41}$:$CURR_{43}$, RGB_1,RGB2,RGB_3(VANA2).
V_{IN_LV}	3.3V Pins	-0.3	5.0	V	Applicable for 3.3V pins VDD_GPIO; GPIO0:GPIO2; GPI; serial interface pins CLK, DATA; V_{2_5}; RBIAS, CREF
I_{IN}	Input Pin Current	-25	+25	mA	At 25ºC, Norm: JEDEC 17
T_{strg}	Storage Temperature Range	-55	125	ºC	
	Humidity	5	85	%	Non-condensing
V_{ESD}	Electrostatic Discharge	-1000	1000	V	Norm: MIL 883 E Method 3015
P_t	Total Power Dissipation QFN32 5x5		1	W	TA = 70 degrees, Tjunction max = 125deg
			2.5	W	TA = 70 degrees, Tjunction max = 125deg; for 800ms
T_{BODY}	Peak Body Temperature		260	ºC	T = 20 to 40s, in accordance with *IPC/JEDEC J-STD 020C.*

5.2 Operating Conditions

Table 2 – Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{HV}	High Voltage	0.0		15.0	V	Applicable for high-voltage current sink pins $CURR_1$ and $CURR_2$.
V_{BAT}	Battery Voltage	3.0	3.6	5.5		V_{BAT1}:V_{BAT3}
V_{GPIO}	Periphery Supply Voltage	1.5		3.3	V	For GPIO and serial interface pins.
V_{2_5}	Voltage on Pin V_{2_5}	2.4	2.5	2.6	V	Internally generated
T_{AMB}	Operating Temperature Range	-30	25	85	°C	
I_{ACTIVE}	Battery current		64	130	µA	Normal Operating current – see section 'Operating Modes' (excluding current of the enabled blocks, e.g. LDOs, DCDC); interface active

Symbol	Parameter	Min	Typ	Max	Unit	Note
$I_{LOWPOWER}$	Low-Power Mode Current		10	18	µA	Current consumption in low-power mode; **ldo_ana1_lpo**= 1, **ldo_ana1_on=1 and V_{2_5} on,** maximum LDO load current on ldo_ana1 = 5mA; interface active
$I_{STANDBY}$	Standby Mode Current		8	13	µA	Current consumption in standby mode. Only 2.5V regulator on V_{DD_GPIO} > 1.5V; interface active
$I_{SHUTDOWN}$	Shutdown Mode Current		0.1	3	µA	V_{DD_GPIO} < 0.3V; interface disabled and register are reset

Notes:

1. All device parameters are valid under all operating conditions unless otherwise specified

6 Typical Operating Characteristics

Figure 2 – DCDC Step Up Converter: Efficiency at VBAT = 3.8V

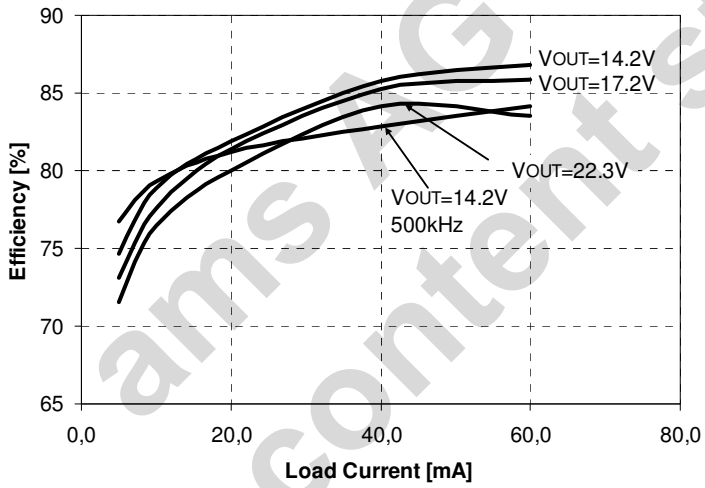


Figure 3 – Charge Pump: Efficiency vs. VBAT

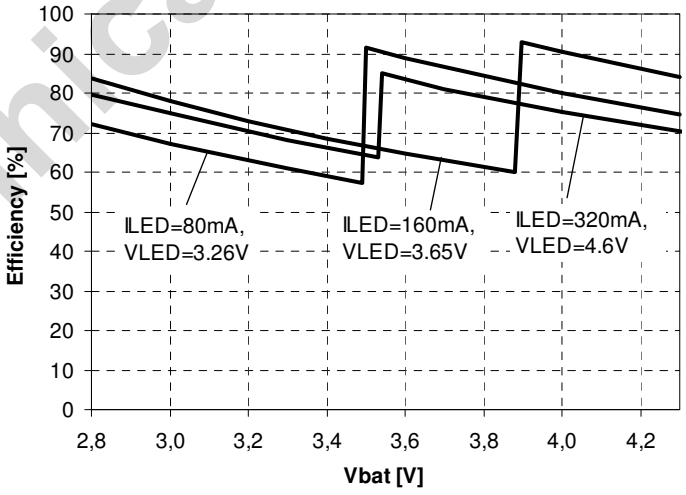


Figure 4 – Charge Pump: Battery Current vs. VBAT

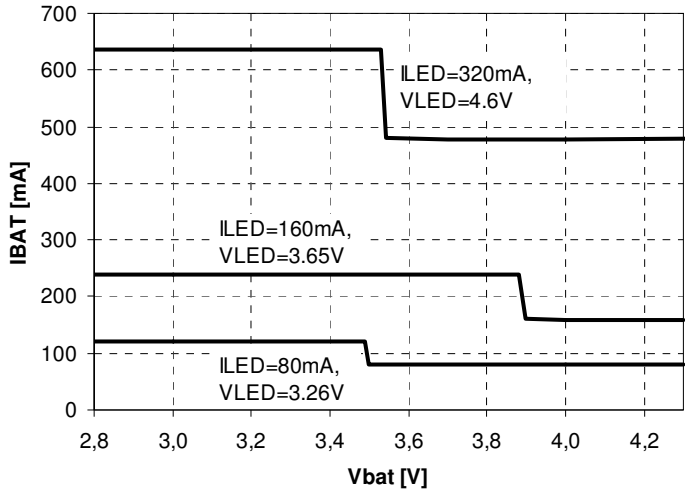


Figure 5 – Current Sink CURR1 vs. V(CURR1)

Figure 6 – Current Sink CURR1 Protection Current vs. Voltage (I(CURR1)=0mA)

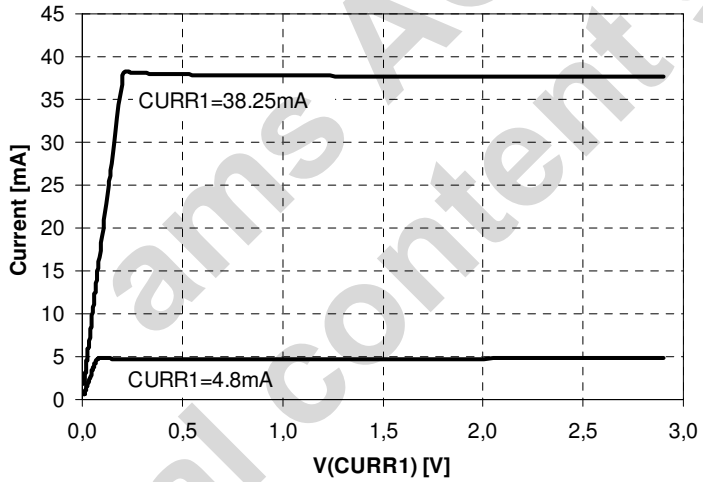
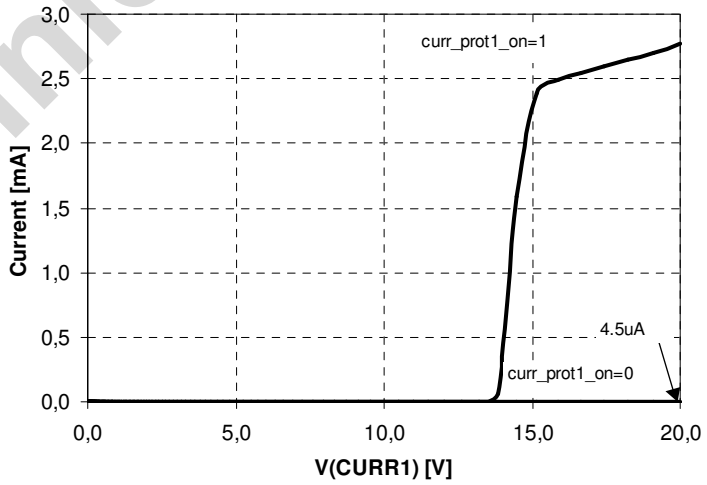


Figure 7 – Current Sink CURR30 vs. V(CURR30)



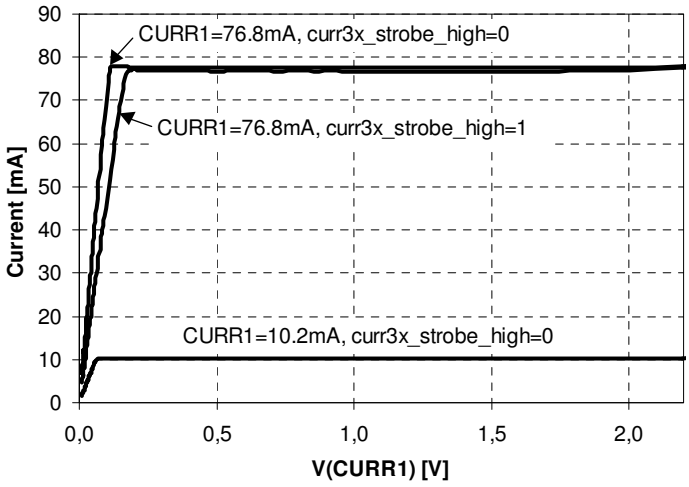
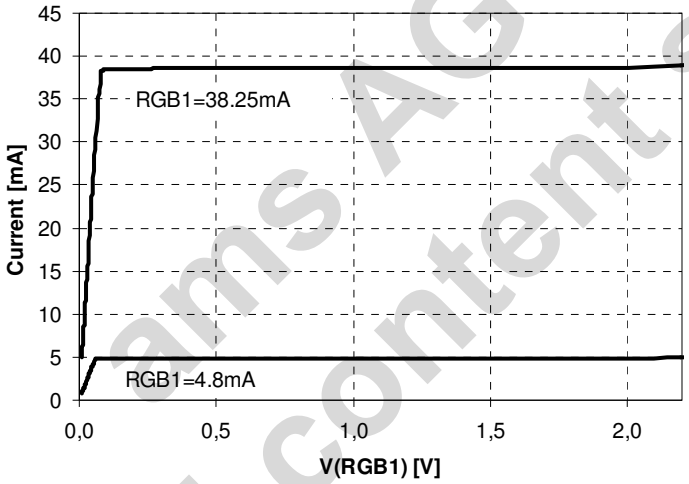


Figure 8 – RGB Current Sinks RGB1 vs. V(RGB1)



7 Detailed Functional Description

7.1 Analog LDO

The Analog LDOs (V_{ANA1}, V_{ANA2}) is designed to supply power to sensitive analog circuits like camera supply, LNAs, Transceivers, VCOs, and other critical RF components of cellular radios. Additionally, the Analog LDO is suitable for supplying power to audio devices or as a reference for A/D and D/A converters.
The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices.
Stability is guaranteed with ceramic output capacitors (see Figure 3) of 1µF ±20% (X5R) or 2.2µF +100/-50% (Z5U). The low ESR of these capacitors ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress ripple on the battery caused by the PA in TDMA systems. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power transistor enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease in performance.
The LDO is off by default after startup (apply voltage on V_{DD_GPIO})

Figure 9 – Analog LDO Block Diagram

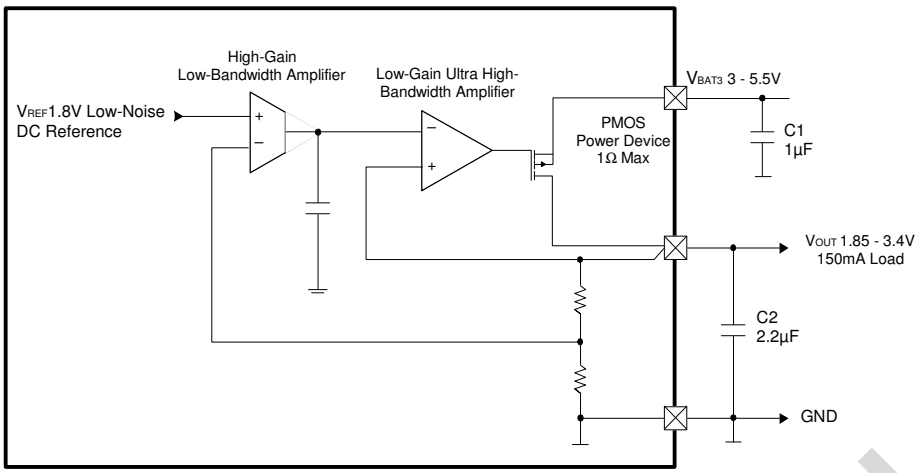


Table 3 – Analog LDOs Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{BAT}	Supply Voltage Range	3.0		5.5	V	
R_{ON}	On Resistance			1.0	Ω	@150mA, full operating temperature range
$V_{DROPOUT}$	Dropout Voltage			150	mV	@150mA, **ldo_ana1_lpo**= 0
				50	mV	@50mA, **ldo_ana1_lpo**= 0
				500	mV	@5mA, **ldo_ana1_lpo**= 1
P_{SRR}	Power Supply Rejection Ratio	70			dB	f = 1kHz, Iout=10mA,V_{BAT}-$V_{ANA1,2}$=0.2V
		55			dB	f = 10kHz Iout=10mA,V_{BAT}-$V_{ANA1,2}$=0.2V
		40			dB	f = 100kHz Iout=10mA,V_{BAT}-$V_{ANA1,2}$=0.2V
I_{On}	Supply Current		50		µA	Without load
			3			Without load, **ldo_ana1_lpo**= 1 **ldo_ana1 only**
			150			With 150mA load
I_{OFF}	Shutdown Current			100	nA	Without load
Noise	Output noise			50	µVrms	10Hz < f < 100kHz
t_{start}	Startup Time			200	µs	
V_{out_tol}	Output Voltage Tolerance	-2		+2	%	**ldo_ana1_lpo**= 0
V_{out}	Output Voltage	1.85		2.85	V	V_{BAT} > 3.0V
		1.85		3.4	V	Full Programmable Range
$V_{LineReg}$	Line Regulation **ldo_ana1_lpo**= 0	-1		+1	mV	Static (1)
		-10		+10	mV	Transient; Slope: t_r = 10µs (1)
		-3		+3	mV	Transient; Slope: t_r = 30µs (V_{BAT}-$V_{ANA1,2}$) >500mV, Iout=1mA
$V_{LoadReg\_HP}$	Load Regulation **ldo_ana1_lpo**= 0	-1		+1	mV	Static (2)
		-20		+20	mV	Transient; Slope: t_r = 10µs (3)
		-8		+8	mV	Transient; Slope: t_r = 30µs (3)

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{LIMIT}[8]	LDO Current Limit **ldo_ana1_lpo**= 0	300	450[7]	520[7]	mA	Pin VANA1. LDO acts as current source if the output current exceeds I_{LIMIT}. (6)
		300	450[7]	520[7]	mA	Pin VANA2
	LDO Current Limit **ldo_ana1_lpo**= 1	4	8		mA	VBAT3-VANA>=0.2V
$V_{LoadReg\_LP}$	Load Regulation **ldo_ana1_lpo**= 1	-10		10	mV	Static (4)
		-50		50	mV	Transient; Slope: t_r = 10µs (5)

Notes:

1. The Line Regulation in Table 3 is valid for whole output voltage (1.8 to 3.3V), if (V_{BAT}-$V_{ANA1,2}$) >200mV.
2. The static Load Regulation in Table 3 is valid for whole output voltage (1.8 to 3.3V) and current range (0 to 100mA), if (V_{BAT}-$V_{ANA1,2}$) >200mV.
3. The load condition for this value is a 1 to 100mA and 100 to 1mA steps.
4. The static load regulation in Table 3 is valid for the whole output voltage range (1.8 to 3.3V) and current range (0 to 5mA), if (V_{BAT}-$V_{ANA1,2}$) >500mV.
5. The load condition for this value is a 0.05 to 5mA and 5 to 0.05mA steps.
6. The duration of operation in current limit is only dependent on the total power dissipation of the device. If this limit exceeded, the overtemperature detection might disable the device temporarily.
7. During startup of the LDO the current limit is half the value of I_{LIMIT}
8. Not production tested – guaranteed by design and laboratory verification

7.1.1 LDO Registers

Table 4 – Register definition for Analog LDO

Addr: 00		**Reg. Control**		
		This register enables/disables the LDOs, Charge Pumps, Charge Pump LEDs, current sinks, the Step Up DC/DC Converter, and low-power mode.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	ldo_ana1_on	0	R/W	0 = Analog LDO is switched off 1 = Analog LDO is switched on
1	ldo_ana2_on	0	R/W	0 = Analog LDO is switched off 1 = Analog LDO is switched on
7	ldo_ana1_lpo	0	R/W	0 = Normal Operation 1 = Low-power mode; **(ldo_ana1 only),**current consumption is reduced by about 75µA. Reduced performance of LDO: max 5mA load, internal oscillator is switched off. The device will exit low-power mode automatically, if blocks requiring the oscillator are enabled.

Table 5 – Register definition for Analog LDO

Addr: 07h		Ldo ana1 voltage		
		This register sets the output voltage (VANA) for the LDO.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
4:0	ldo_ana1_voltage	00000b	R/W	Controls LDO voltage selection. 00000b = 1.85V. ... LSB = 50mV 11111b = 3.4V

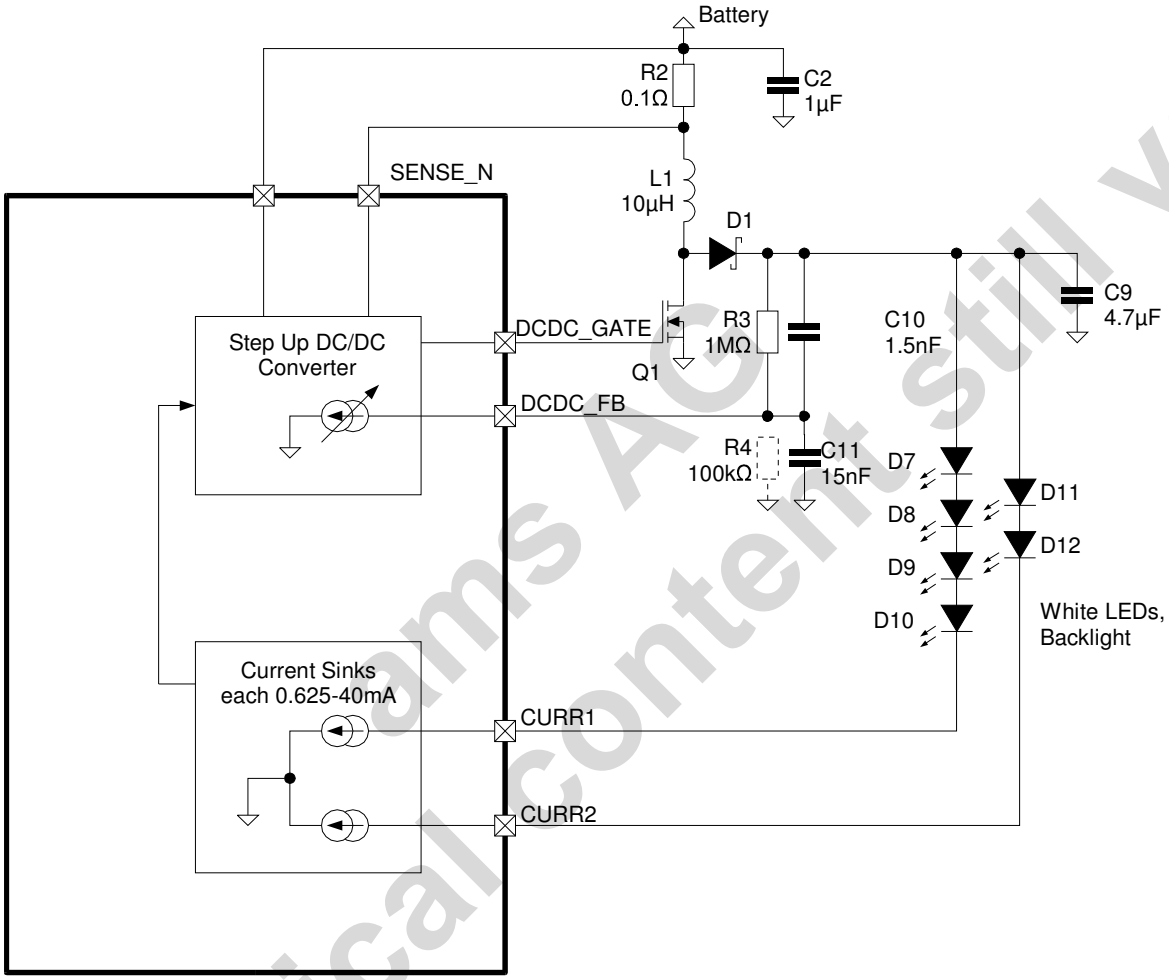
Table 6 – Register definition for Analog LDO

Addr: 08h		Ldo ana2 voltage		
		This register sets the output voltage (VANA) for the LDO.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
4:0	ldo_ana2_voltage	00000b	R/W	Controls LDO voltage selection. 00000b = 1.85V. ... LSB = 50mV 11111b = 3.4V
5	ldo_ana2_pulld	0	R/W	Enable a pulldown for LDO ANA2 (pin RGB3). If RGB3 current sink or the external charge pump is used, leave this bit at default 0; if the LDO ANA2 is used in a system, set this bit always to 1 0 = pulldown is disabled 1 = pulldown is enabled; has only effect if LDO ANA2 is off (ldo_ana2_on = 0)

7.2 Step Up DC/DC Converter

The DCDC step up converter is only available in the AS3688 version (not available for the AS3688B – marking 'AS3688B').
The Step Up DC/DC Converter is a high-efficiency current mode PWM regulator, providing output voltage up to 25V and a load current up to 50mA. A constant switching-frequency results in a low noise on the supply and output voltages.

Figure 10 – Step Up DCDC Converter Block Diagrammö Option: Current Feedback with Overvoltage protection



TBD: Final Datasheet: Add internal logic with overvoltage detection.

Table 7 – Step Up DC/DC Converter Parameters

Symbol	Parameter	Min	TYP	Max	Unit	Note
IVDD	Quiescent Current		140		µ A	Pulse skipping mode.
VFB1	Feedback Voltage for External Resistor Divider	1.20	1.25	1.30	V	For constant voltage control. **step_up_res=1**
VFB2	Feedback Voltage for Current Sink Regulation	0.4	0.5	0.6	V	on CURR1 or CURR2 in regulation. **step_up_res=0**
IDCDC_FB	Additional Tuning Current at Pin DCDC_FB and overvoltage protection	0		30	µ A	Adjustable by software using Register DCDC control1 1µA step size $V_{PROTECT}$ = 1.25V + I_{DCDC_FB} * R_3 Design Target
	Accuracy of Feedback Current	-4		4	%	
Vrsense_max	Current Limit Voltage at R_{SENSE} (R2)	55	72	93	mV	e.g., 0.66A for 0.1Ω sense resistor.
Vrsense_max_start		27	36	47		For fixed startup time of 500us
Vrsense_max_lc		33	47	61		If stepup_lowcur=1
RSW	Switch Resistance			1	Ω	ON-resistance of external switching transistor.
Iload	Load Current	0		50	mA	At 15V output voltage.
				45	mA	At 17V output voltage.
fIN	Switching Frequency	0.9	1	1.1	MHz	Internally trimmed.
Cout	Output Capacitor	0.7	4.7		µ F	Ceramic, ±20%. Use nominal 2.2µF capacitors to obtain at least 0.7µF under all conditions (voltage dependance of capacitors)
L	Inductor	7	10	13	µ H	Use inductors with small $C_{parasitic}$ (<100pF) to get high efficiency.
tMIN_ON	Minimum on Time	90	140	190	ns	
MDC	Maximum Duty Cycle	88	91		%	
Vripple	Voltage ripple >20kHz			160	mV	Cout=2.2uF,Iout=0..45mA, Vbat=3.0...4.2V
	Voltage ripple <20kHz			40	mV	
Efficiency	Efficiency		85		%	Iout=20mA,Vout=17V,Vbat=3.8V

To ensure soft startup of the dcdc converter, the overcurrent limits are reduced for a fixed time after enabling the dcdc converter. The total startup time for an output voltage of e.g. 25V is less than 2ms.

7.2.1 Feedback Selection

Register 12 (DCDC Control) selects the type of feedback for the Step Up DC/DC Converter.

The feedback for the DC/DC converter can be selected either by current sinks CURR1 or CURR2 or by a voltage feedback at pin DCDC_FB. If the register bit step_up_fb_auto is set, the feedback path is automatically selected between CURR1 and CURR2 (the lowest voltage of these current sinks is used).

Setting step_up_fb = 01 enables feedback at pin 19 (CURR1); setting step_up_fb = 10 enables feedback at pin 20 (CURR2). The Step Up DC/DC Converter is regulated such that the required current at the feedback path can be supported. (Bit step_up_res should be set to 0 in this configuration)

Note: Always choose the path with the higher voltage drop as feedback to guarantee adequate supply for the other (unregulated) path or enable the register bit step_up_fb_auto.

7.2.2 Overvoltage Protection in Current Feedback Mode

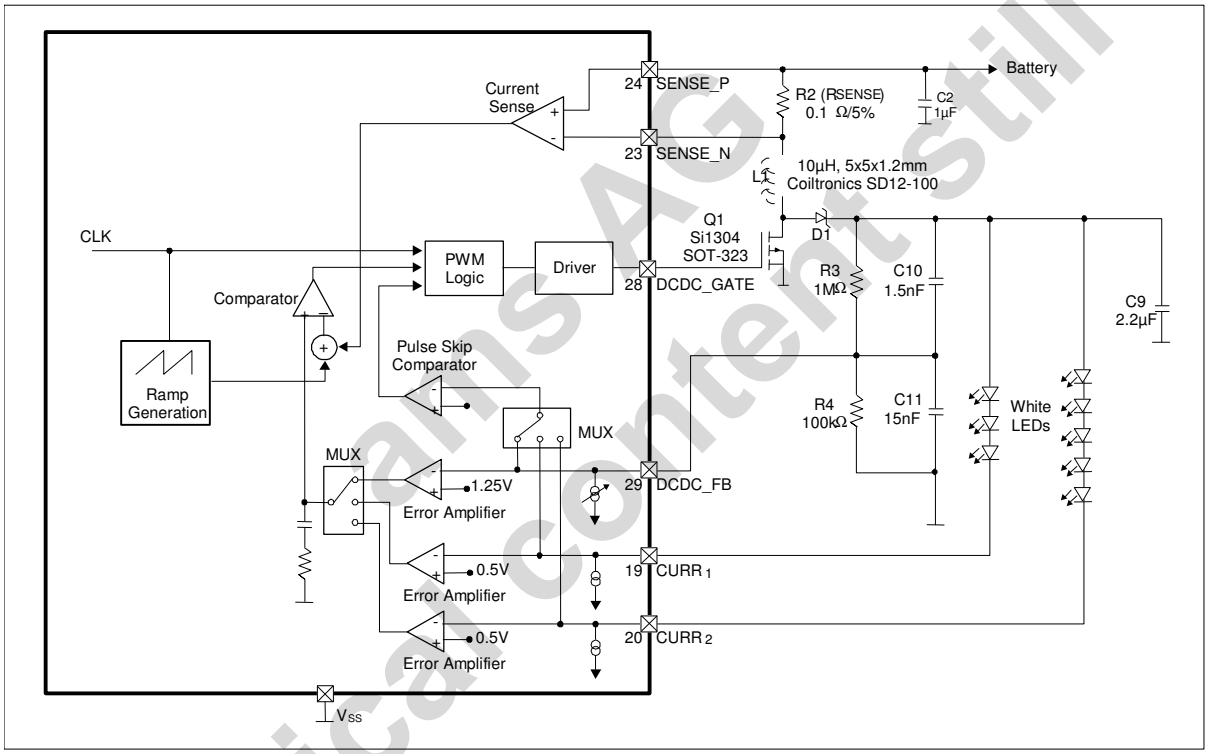
The overvoltage protection in current feedback mode (step_up_fb = 01 or 10) works as follows: Only resistor R3 and C10 is soldered and R4 and C11 is omitted. An internal current source (sink) is used to generate a voltage drop across the resistor R3. If then the voltage on DCDC_FB is above 1.25V, the DCDC is momentarily disabled to avoid too high voltages on the output of the DCDC converter.
The protection voltage can be calculated according to the following formula:

$$V_{PROTECT} = 1.25V + I_{DCDC\_FB} * R_3$$

Notes:

1. The voltage on the pin DCDC_FB is limited by an internal protection diode to VBAT + one diode forward voltage (typ. 0.6V).
2. If the overvoltage protection is not used in current feedback mode, connect DCDC_FB to ground.

Figure 11 –Step Up DC/DC Converter Block Diagram; Option: Regulated Output Voltage, Feedback is at Pin DCDC_FB



7.2.3 Voltage Feedback

Setting bit step_up_fb = 00 enables voltage feedback at pin DCDC_FB..

The output voltage is regulated to a constant value, given by (Bit step_up_res should be set to 1 in this configuration)

$$U_{stepup\_out} = (R3+R4)/R4 \times 1.25 + I_{DCDC\_FB} \times R3$$

If R4 is not used, the output voltage is by (Bit step_up_res should be set to 0 in this configuration):

$$U_{stepup\_out} = 1.25 + I_{DCDC\_FB} \times R3$$

Where:

U_{stepup_out} = Step Up DC/DC Converter output voltage.

R3 = Feedback resistor R3.

R4 = Feedback resistor R4.

I_{DCDC_FB} = Tuning current at pin 29 (DCDC_FB); 0 to 31µA.

Table 8 – Voltage Feedback Example Values

$I_{vtuning}$	U_{stepup_out}	U_{stepup_out}
µ A	R3 = 1MΩ, R4 not used	R3 = 500kΩ, R4 = 50kΩ
0	-	13.75
1	-	14.25
2	-	14.75
3	-	15.25
4	-	15.75
5	6.25	16.25
6	7.25	16.75
7	8.25	17.25
8	9.25	17.75
9	10.25	18.25
10	11.25	18.75
11	12.25	19.25
12	13.25	19.75
13	14.25	20.25
14	15.25	20.75
15	16.25	21.25
…	…	…
30	31.25	28.75
31	32.25	29.25

Caution: The voltage on CURR1 and CURR2 must not exceed 15V – see also section 'High Voltage Current Sinks'.

7.2.4 PCB Layout Tips

To ensure good EMC performance of the DCDC converter, keep its external power components C2, R2, L1, Q1, D1 and C9 close together. Connect the ground of C2, Q1 and C9 locally together and connect this path with a single via to the main ground plane. This ensures that local high-frequency currents will not flow to the battery.

7.2.5 Step up Registers

Addr: 00		Reg. Control		
		This register enables/disables the LDOs, Charge Pumps, Charge Pump LEDs, current sinks, the Step Up DC/DC Converter		
Bit	**Bit Name**	**Default**	**Access**	**Description**
3	step_up_on	0	R/W	Enable the step up converter 0b = Disable the Step Up DC/DC Converter. 1b = Enable the Step Up DC/DC Converter.

Addr: 21h		DCDC Control 1		
		This register controls the Step Up DC/DC Converter.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	step_up_frequ	0	R/W	Defines the clock frequency of the Step Up DC/DC Converter. 0 = 1 MHz 1 = 500 kHz
2:1	step_up_fb	00	R/W	Controls the feedback source if step_up_fb_auto = 0 00 = DCDC_FB enabled (external resistor divider). Set step_up_fb=00 (DCDC_FB), if external PWM is enabled for CURR1 or CURR2 01 = CURR1 feedback enabled (feedback via white LEDs. 10 = CURR2 feedback enabled (feedback via white LEDs. 11 = Reserved.
7:3	step_up_vtuning	00000	R/W	Defines the tuning current at pin DCDC_FB. 00000 = 0 µA 00001 = 1 µA 00010 = 2 µA … 10000 = 15 µA … 11111 = 31 µA

Addr: 22h		DCDC Control 2		
		This register controls the Step Up DC/DC Converter and low-voltage current sinks CURR3x.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	step_up_res	0	R/W	Gain selection for Step Up DC/DC Converter. 0 = Select 0 if Step Up DC/DC Converter is used with current feedback (CURR1, CURR2) or if DCDC_FB is used with current feedback only – only R1, C1 connected 1 = Select 1 if DCDC_FB is used with external resistor divider (2 resistors).
1	skip_fast	0	R/W	Step Up DC/DC Converter output voltage at low loads, when pulse skipping is active. 0 = Accurate output voltage, more ripple. 1 = Elevated output voltage, less ripple.
2	stepup_prot	1	R/W	Step Up DC/DC Converter protection. 0 = No overvoltage protection. 1 = Overvoltage protection on pin DCDC_FB enabled voltage limitation =1.25V on DCDC_FB

Addr: 22h		DCDC Control 2		
		This register controls the Step Up DC/DC Converter and low-voltage current sinks CURR3x.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
3	stepup_lowcur	1	R/W	Step Up DC/DC Converter coil current limit. 0 = .Normal current limit 1 = Current limit reduced by approx. 33%
4	curr1_prot_on	0	R/W	0 = No overvoltage protection 1 = Pull down current on CURR1 switched on, if voltage on CURR1 exceeds 13.75V, and step_up_on=1
5	curr2_prot_on	0	R/W	0 = No overvoltage protection 1 = Pull down current on CURR1 switched on, if voltage on CURR1 exceeds 13.75V, and step_up_on=1
7	step_up_fb_auto	0	R/W	0 = step_up_fb select the feedback of the DCDC converter 1 = The feedback is automatically chosen within the current sinks CURR1and CURR2 (never DCDC_FB). Only those are used for this selection, which are enabled (currX_mode must not be 00) and not connected to the charge pump (currX_on_cp must be 0). Don't use automatic feedback selection together with external PWM for CURR1 or CURR2.

7.3 Charge Pump

The Charge Pump uses two external flying capacitors C6, C7 to generate output voltages higher than the battery voltage.
There are three different operating modes of the charge pump itself:

- 1:1 Bypass Mode
  - Battery input and output are connected by a low-impedance switch (0.5Ω);
  - battery current = output current.
- 1:1.5 Mode
  - The output voltage is up to 1.5 times the battery voltage (without load), but is limited to VCPOUTmax all the time
  - battery current = 1.5 times output current.
- 1:2 Mode
  - The output voltage is up to 2 times the battery voltage (without load), but is limited to VCPOUTmax all the time
  -
  - battery current = 2 times output current

As the battery voltage decreases, the Charge Pump must be switched from 1:1 mode to 1:1.5 mode and eventually in 1:2 mode in order to provide enough supply for the current sinks. Depending on the actual current the mode with best overall efficiency can be automatically or manually selected:

Examples:

- Battery voltage = 3.7V, LED dropout voltage = 3.5V. The 1:1 mode will be selected and there is 100mV drop on the current sink and on the Charge Pump switch. Efficiency 95%.
- Battery voltage = 3.5V, LED dropout voltage = 3.5V. The 1:1.5 mode will be selected and there is 1.5V drop on the current sink and 250mV on the Charge Pump. Efficiency 66%.
- Battery voltage = 3.8V, LED dropout voltage = 4.5V (Camera Flash). The 1:2 mode can be selected and there is 600mV drop on the current sink and 2.5V on the Charge Pump. Efficiency 60%.

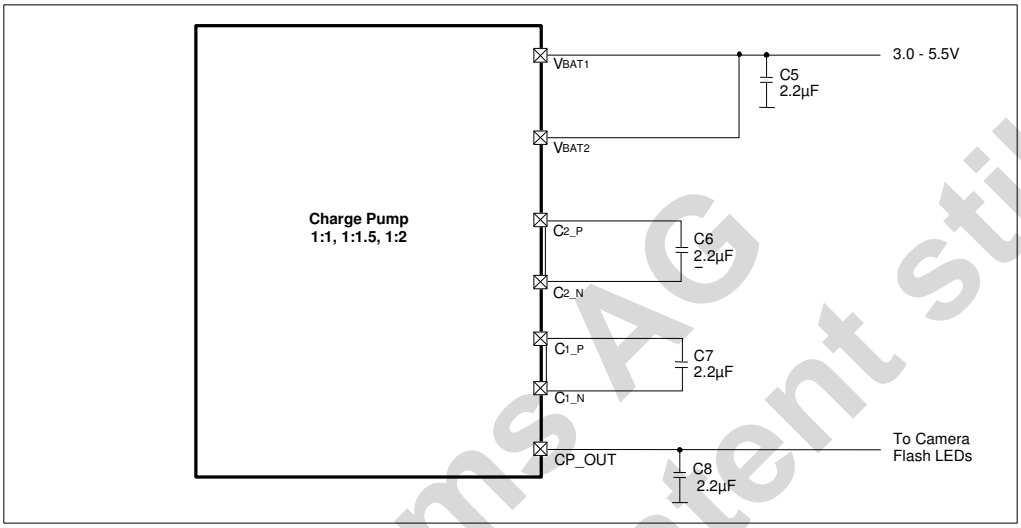
The efficiency is dependent on the LED forward voltage given by:

$$Eff=(V\_LED*Iout)/(U_{in}*I_{in})$$

The charge pump mode switching can be done manually or automatically with the following possible software settings:

- Automatic up all modes allowed (1:1, 1:1.5, 1:2)
  - Start with 1:1 mode
  - Switch up automatically 1:1 to 1:1.5 to 1:2
- Automatic up, but only 1:1 and 1:1.5 allowed
  - Start with 1:1 mode
  - Switch up automatically only from 1:1 to 1:1.5 mode; 1:2 mode is not used
- Manual
  - Set modes 1:1, 1:1.5, 1:2 by software

Figure 12 – Charge Pump Pin Connections



The Charge Pump requires the external components listed in the following table:

Table 9 – Charge Pump External Components

Symbol	Parameter	Min	Typ	Max	Unit	Note
C_6, C_7	External Flying Capacitor (2x)	0.65 (@3.2V, 1MHz)	2.2		µ F	Ceramic low-ESR capacitor between pins C1_P and C1_N, and between pins C2_P and C2_N. Use nominal 2.2µF capacitors (size 0603)
C_5	Supply Buffer Capacitor	1.0 (@3.3V)	2.2		µ F	Ceramic low-ESR capacitor between pins CP_OUT and VSS, pins VBAT and VBAT2 (in parallel) and VSS. Use nominal 2.2µF capacitors (size 0603)
C_8	External Storage Capacitor	1.5	2.2 or 4.7		µ F	Ceramic low-ESR capacitor between pins CP_OUT and VSS, pins VBAT and VBAT2 (in parallel) and VSS. Use nominal 2.2µF or 4.7µF capacitors (size 0603)

Note:

1.) The connections of the external capacitors C5, C6, C7 and C8 should be kept as short as possible.

2.) The maximum voltage on the flying capacitors C6 and C7 is VBAT

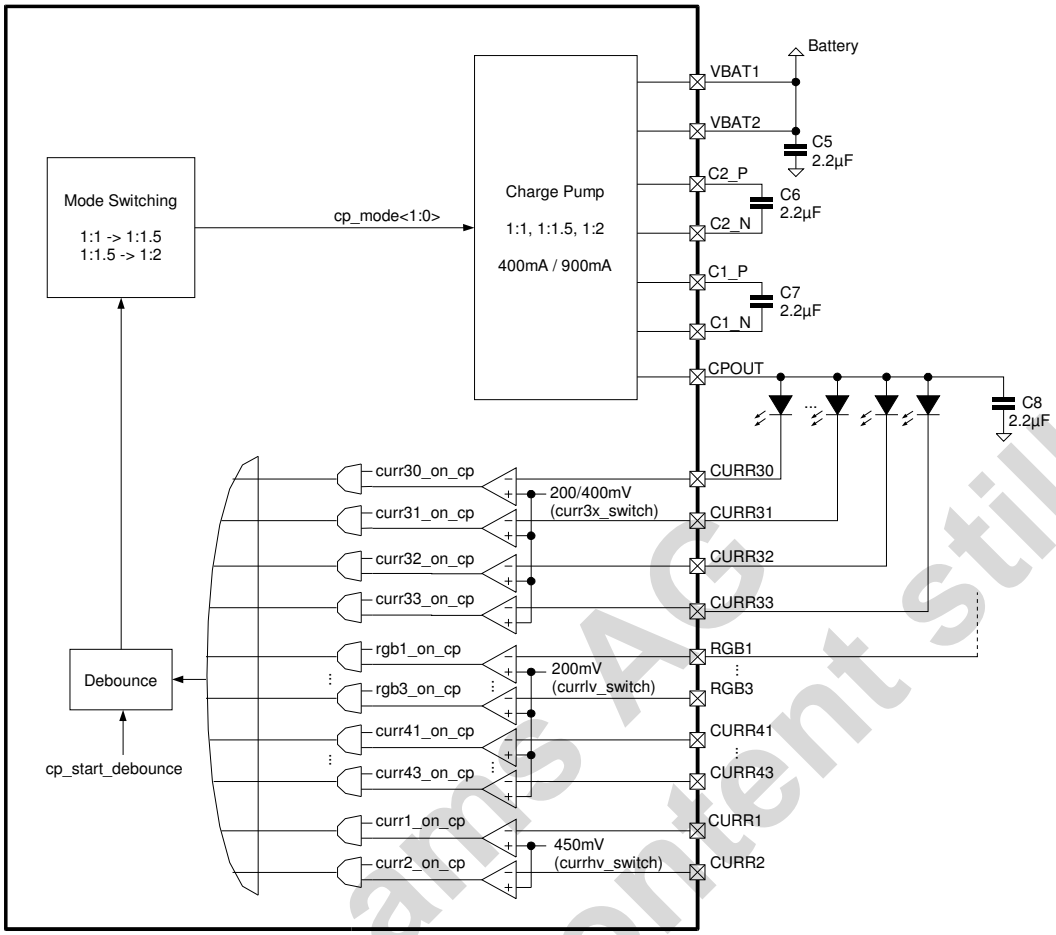
Table 10 – Charge Pump Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
ICPOUT_Pulsed	Output Current Pulsed	0.0		900	mA	300ms pulse width, 10% duty cycle max.
ICPOUT	Output Current Continuous	0.0		400	mA	
VCPOUTmax	Output Voltage			5.6	V	Internally limited, Including output ripple
η	Efficiency	55		90	%	Including current sink loss; ICPOUT < 400mA.
$I_{CP1\_1.5}$	Power Consumption without Load fclk = 1 MHz		8.4	13	mA	1:1.5 Mode
I_{CP1_2}			9.5	18		1:2 Mode
R_{cp1_1}	Effective Charge Pump Output Resistance (Open Loop, fclk = 1MHz)		0.4	1.0	Ω	1:1 Mode; V_{BAT} >= 3.5V
$R_{cp1\_1.5}$			1.4	2.0		1:1.5 Mode; V_{BAT} >= 3.3V ; $T_{JUNCTION}$<85°C
R_{cp1_2}			1.8	2.5		1:1.2 Mode; V_{BAT} >= 3.1V
fclk Accuracy	Accuracy of Clock Frequency	-10		10	%	
currlv_switch	RGB1:RGB3 and CURR41:CURR42 minumum voltage			0.2	V	If the voltage drops below this threshold, the charge pump will use the next available mode (1:1 -> 1:1.5 or 1:1.5 -> 1:2)
currhv_switch	CURR1, CURR2 minumum voltage			0.45	V	
curr3x_switch	CURR30:CURR33 minumum voltage 0-160mA range			0.2	V	
	CURR30:CURR33 minumum voltage >160mA range			0.4	V	
t_{deb}	CP automatic up-switching debounce time		240		µsec	

7.3.1 Charge Pump Mode Switching

If automatic mode switching is enabled (cp_mode_switching = 00 or cp_mode_switching = 01) the charge pump monitors the current sinks, which are connected via a led to the output CP_OUT. To identify these current sources (sinks), the registers cp_mode_switch1 and cp_mode_switch2 (register bits curr30_on_cp … curr33_on_cp, rgb1_on_cp … rgb3_on_cp, curr1_on_cp, curr2_on_cp, curr41_on_cp … curr43_on_cp) should be setup before starting the charge pump (cp _on = 1). If any of the voltage on these current sources drops below the threshold (currlv_switch, currhv_switch, curr3x_switch), the next higher mode is selected after the debounce time.
To avoid switching into 1:2 mode (battery current = 2 times output current), set cp_mode_switching = 10.
If the currX_on_cp=0 and the according current sink is connected to the chargepump, the current sink will be functional, but there is no up switching of the chargepump, if the voltage compliance is too low for the current sink to supply the specified current.

Figure 13 – Automatic Mode Switching



7.3.2 Soft Start

An implemented soft start mechanism reduces the inrush current. Battery current is smoothed when switching the charge pump on and also at each switching condition. This precaution reduces electromagnetic radiation significantly.

7.3.3 Charge Pump Registers

Addr: 00h		**Reg. Control**		
		This register enables/disables the LDOs, Charge Pumps, Charge Pump LEDs, current sinks, the Step Up DC/DC Converter.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2	cp _on	0	R/W	0 = Set Charge Pump into 1:1 mode (off state) unless cp_auto_on is set 1 = Enable manual or automatic mode switching – see register CP Control for actual settings

Addr: 23h		CP Control		
		This register controls the Charge Pump.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	cp_clk	0	R/W	Clock frequency selection. 0 = 1 MHz 1 = 500 kHz
2:1	cp_mode	00b	R/W	Charge Pump mode (in manual mode sets this mode, in automatic mode reports the actual mode used) 00 = 1:1 mode 01 = 1:1.5 mode 10 = 1:2 mode 11 = NA **Note:** Direct switching from 1:1.5 mode into 1:2 in manual mode and vice versa is not allowed. Always switch over 1:1 mode.
4:3	cp_mode_switching	00b	R/W	Set the mode switching algorithm: 00 = Automatic Mode switching; 1:1, 1:1.5 and 1:2 allowed[1] 01 = Automatic Mode switching; only 1:1 and 1:1.5 allowed[1] 10 = Manual Mode switching; register cp_mode defines the actual charge pump mode used 11 = reserved
6	cp_auto_on	0	R/W	0 = Charge Pump is switched on/off with cp _on 1 = Charge Pump is automatically switched on if a current sink, which is connected to the charge pump (defined by registers CP Mode Switch 1 & 2) is switched on

Note :

1. Don't use automatic mode switching together with external PWM for the current sources connceted to the charge pump with less than 500us high time.

Addr: 24h		CP Mode Switch 1		
		Setup which current sinks are connected (via leds) to the charge pump; if set to '1' the correspond current source (sink) is used for automatic mode selection of the charge pump		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr30_on_cp	0	R/W	0 = current Sink CURR30 is not connected to charge pump 1 = current sink CURR30 is connected to charge pump
1	curr31_on_cp	0	R/W	0 = current Sink CURR31 is not connected to charge pump 1 = current sink CURR31 is connected to charge pump
2	curr32_on_cp	0	R/W	0 = current Sink CURR32 is not connected to charge pump 1 = current sink CURR32 is connected to charge pump
3	curr33_on_cp	0	R/W	0 = current Sink CURR33 is not connected to charge pump 1 = current sink CURR33 is connected to charge pump
4	rgb1_on_cp	0	R/W	0 = current Sink RGB1 is not connected to charge pump 1 = current sink RGB1 is connected to charge pump
5	rgb2_on_cp	0	R/W	0 = current Sink RGB2 is not connected to charge pump 1 = current sink RGB2 is connected to charge pump
6	rgb3_on_cp	0	R/W	0 = current Sink RGB3 is not connected to charge pump 1 = current sink RGB3 is connected to charge pump
7				NA

Addr: 25h		CP Mode Switch 2		
		Setup which current sinks are connected (via leds) to the charge pump; if set to '1' the correspond current source (sink) is used for automatic mode selection of the charge pump		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr1_on_cp	0	R/W	0 = current Sink CURR1 is not connected to charge pump 1 = current sink CURR1 is connected to charge pump
1	curr2_on_cp	0	R/W	0 = current Sink CURR2 is not connected to charge pump 1 = current sink CURR2 is connected to charge pump
2	curr41_on_cp	0	R/W	0 = current Sink CURR41 is not connected to charge pump 1 = current sink CURR41 is connected to charge pump
3	curr42_on_cp	0	R/W	0 = current Sink CURR42 is not connected to charge pump 1 = current sink CURR42 is connected to charge pump
4	curr43_on_cp	0	R/W	0 = current Sink CURR43 is not connected to charge pump 1 = current sink CURR43 is connected to charge pump

Addr: 2Ah		Curr low voltage status 1		
		Indicates the low voltage status of the current sinks. If the currX_low_v bit is set, the voltage on the current sink is too low, to drive the selected output current		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr30_low_v	NA	R	0 = voltage of current Sink CURR30 >curr3x_switch 1 = voltage of current Sink CURR30 <curr3x_switch
1	curr31_low_v	NA	R	0 = voltage of current Sink CURR31 >curr3x_switch 1 = voltage of current Sink CURR31 <curr3x_switch
2	curr32_low_v	NA	R	0 = voltage of current Sink CURR32 >curr3x_switch 1 = voltage of current Sink CURR32 <curr3x_switch
3	curr33_low_v	NA	R	0 = voltage of current Sink CURR33 >curr3x_switch 1 = voltage of current Sink CURR33 <curr3x_switch
4	rgb1_low_v	NA	R	0 = voltage of current Sink RGB1 >currlv_switch 1 = voltage of current Sink RGB1 <currlv_switch
5	rgb2_low_v	NA	R	0 = voltage of current Sink RGB2 >currlv_switch 1 = voltage of current Sink RGB2 <currlv_switch
6	rgb3_low_v	NA	R	0 = voltage of current Sink RGB3 >currlv_switch 1 = voltage of current Sink RGB31 <currlv_switch
7				NA

Addr: 2Bh		Curr low voltage status 2		
		Indicates the low voltage status of the current sinks. If the currX_low_v bit is set, the voltage on the current sink is too low, to drive the selected output current		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr1_low_v	NA	R	0 = voltage of current Sink CURR1 >currhv_switch 1 = voltage of current Sink CURR1 <currhv_switch
1	curr2_low_v	NA	R	0 = voltage of current Sink CURR2 >currhv_switch 1 = voltage of current Sink CURR2 <currhv_switch
2	curr41_low_v	NA	R	0 = voltage of current Sink CURR41 >currlv_switch 1 = voltage of current Sink CURR41 <currlv_switch
3	curr42_low_v	NA	R	0 = voltage of current Sink CURR42 >currlv_switch 1 = voltage of current Sink CURR42 <currlv_switch
4	curr43_low_v	NA	R	0 = voltage of current Sink CURR43 >currlv_switch 1 = voltage of current Sink CURR43 <currlv_switch

7.3.4 Usage of PCB Wire Inductance

The inductance between the battery and pins V_{BAT1} and V_{BAT2} can be used as a filter to reduce disturbance on the battery. Instead of using one capacitor (C5) it is recommended to split C5 into $C5_1$ and $C5_2$ with the capacitance equal:

$$C5_1 = C5_2 = 1/2 \times C5$$

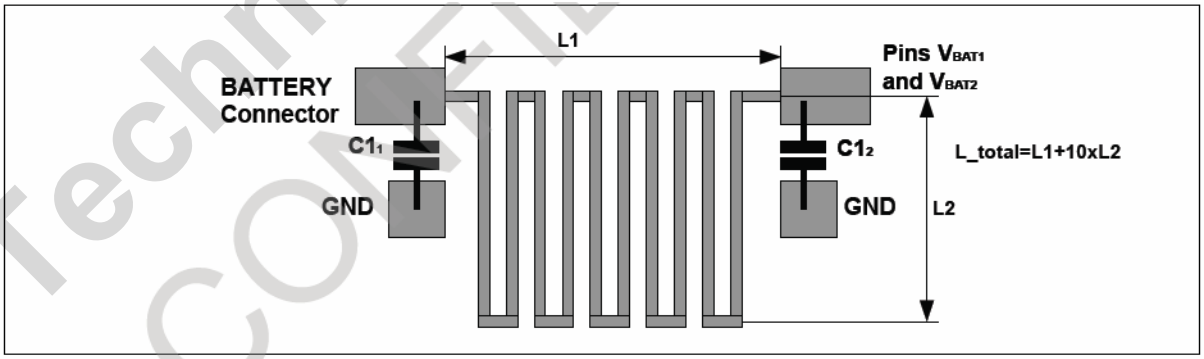
It is recommended to apply a minimum of 20nH (maximum 200nH) with low impedance. This inductance can be realized on the PCB without any discrete coil. Assuming that a 1mm signal line corresponds to approximately 1nH (valid if the length (L) is significantly bigger than the width (W) of the line (L/W <10)), a line length of:

$$20mm < L < 200mm$$

is recommended. The shape of the line is not important.

Figure 14 – PCB Wire Inductance Example 1 (TBD: TODO: replace C1 by C5)

Figure 15 – PCB Wire Inductance Example 2 (TBD: TODO: replace C1 by C5)



7.4 Current Sinks

The AS3688 contains general purpose current sinks intended to control backlights, buzzers, and vibrators. All current sinks have an integrated protection against overvoltage.

CURR1 and CURR2 is also used as feedback for the Step Up DC/DC Converter (regulated to 0.5V in this configuration).

- Current sinks CURR1 and CURR2 are high-voltage compliant (15V) current sinks, used e.g., for series of white LEDs
- Current sinks CURR3*x* (CURR30, CURR31, CURR32 and CURR33) are parallel 5V, high-current current sinks, used e.g., for a photocamera flash LED.
- Current sinks RGB1, RGB2, and RGB3 are general purpose current sinks e.g. for a fun LED (the pins for these current sinks are shared with the OLED charge pump)
- Current sinks CURR4x (CURR41, CURR42, and CURR43) are general purpose current sinks optionally used in place of the Step Up DC/DC Converter, e.g. for white LEDs.

As the current sinks consume current whenever enabled (currX_mode not equal 'off'), do always disable the current sinks by setting their currX_mode register to 'off' (and not by setting currX_current to 0 and not by setting pwm_code to 0 if currX_mode = 'PWM controlled').

Table 11 – Current Sink Function Overview

Current Sink	Pin	Max. Voltage (V)	Max. Current (mA)	Resolution		Software Current Control	Hardware On/Off Control	Alternate Function
				(Bits)	(mA)			
CURR1	TBD	15.0	38.25	8	0.15	Separate	LED Pattern; PWM at GPIO0/2; Internal PWM	N/A
CURR2	TBD							
CURR30	TBD	VBAT (5.5V)	153 (300 for strobe)	8 (+1 for strobe)	0.6	Combined in Strobe/Preview or Separated	Flash LED Strobe (GPI) & Preview (GPIO2); TXMask (GPIO1); PWM at GPIO0/2; Internal PWM; Ext-Overtemp on GPIO2 LED Pattern	
CURR31	TBD							
CURR32	TBD							
CURR33	TBD							
RGB1	TBD		38.25	8	0.15	Separate	LED Pattern; PWM at GPIO0/2; Internal PWM	OLED Charge Pump RGB3: LDO VANA2
RGB2	TBD							
RGB3	TBD							
CURR41	TBD		38.25	8	0.15	Separate	LED Pattern; PWM at GPIO0/2; Internal PWM	Step Up DC/DC Converter (feedback at CURR1 or CURR2)
CURR42	TBD							
CURR43	TBD							

7.4.1 High Voltage Current Sinks CURR1, CURR2

The high voltage current sinks have a resolution of 8 bits. Additionally an internal protection circuit monitors with a voltage divider (max 3µA @ 13V) the voltage on CURR1 and CURR2 and increases the current in off state in case of overvoltage. See section 'Typical Operating Characteristics' Figure 'Current Sink CURR1 and CURR2 Protection Current'. This shows the protection current versus applied voltage depending on the register setting currX_prot_on (X=1 or 2).
External PWM control of these current sinks is possible and can be enabled by software (Input pin GPIO0).

Table 12 – HV - Current Sinks Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{BIT7}	Current sink if Bit7 = 1		19.2		mA	For V(CURRx) > 0.45V
I_{BIT6}	Current sink if Bit6 = 1		9.6			
I_{BIT5}	Current sink if Bit5 = 1		4.8			
I_{BIT4}	Current sink if Bit4 = 1		2.4			
I_{BIT3}	Current sink if Bit3 = 1		1.2			
I_{BIT2}	Current sink if Bit2 = 1		0.6			
I_{BIT1}	Current sink if Bit1 = 1		0.3			
I_{BIT0}	Current sink if Bit0 = 1		0.15			
Δm	matching Accuracy	-8		+8	%	CURR1,CURR2; full scale
Δ	absolute Accuracy	-15		+15	%	
Curr1 – Curr2	Voltage compliance	0.45		15	V	
Ov_prot_ 13V	Overvoltage Protection of current sink CURR1,2			3.0	µA	At 13V, independent of curr1_prot_on or curr2_prot_on
Ov_prot_ 15V	Overvoltage Protection of current sink CURR1,2	0.8		4.0	mA	At 15V, step_up_on=1, curr1_prot_on=1 for CURR1, curr2_prot_on=1 for CURR2

7.4.1.1 High Voltage Current Sinks CURR1, CURR2 Registers

Addr: 09h		**Curr1 current**		
		This register controls the High voltage current sink current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	curr1_current	0	R/W	Defines current into Current sink curr1 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

Addr: 0Ah		**Curr2 current**		
		This register controls the High voltage current sink current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	curr2_current	0	R/W	Defines current into Current sink curr1 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

Addr: 01h		curr12 control		
		This register select the mode of the current sinkscontrols High voltage current sink current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	curr1_mode	0	R/W	Select the mode of the current sink curr1 00b = off 01b = on 10b = PWM controlled 11b = LED pattern controlled; do not use softdim_pattern=1
3:2	curr2_mode	0	R/W	Select the mode of the current sink curr2 00b = off 01b = on 10b = PWM controlled 11b = LED pattern controlled; do not use softdim_pattern=1

Addr: 22h		DCDC Control 2		
		This register controls the Step Up DC/DC Converter and low-voltage current sinks CURR3x.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	step_up_res	0	R/W	Gain selection for Step Up DC/DC Converter. 0 = Select 0 if Step Up DC/DC Converter is used with current feedback (CURR1, CURR2) or if DCDC_FB is used with current feedback only – only R1, C1 connected 1 = Select 1 if DCDC_FB is used with external resistor divider (2 resistors).
1	skip_fast	0	R/W	Step Up DC/DC Converter output voltage at low loads, when pulse skipping is active. 0 = Accurate output voltage, more ripple. 1 = Elevated output voltage, less ripple.
2	stepup_prot	1	R/W	Step Up DC/DC Converter protection. 0 = No overvoltage protection. 1 = Overvoltage protection on pin DCDC_FB enabled voltage limitation =1.25V on DCDC_FB
3	stepup_lowcur	1	R/W	Step Up DC/DC Converter coil current limit. 0 = .Normal current limit 1 = Current limit reduced by approx. 33%
4	curr1_prot_on	0	R/W	0 = No overvoltage protection 1 = Pull down current on CURR1 switched on, if voltage on CURR1 exceeds 13.75V, and step_up_on=1
5	curr2_prot_on	0	R/W	0 = No overvoltage protection 1 = Pull down current on CURR2 switched on, if voltage exceeds on CURR2 13.75V, and step_up_on=1
7	step_up_fb_auto	0	R/W	0 = step_up_fb select the feedback of the DCDC converter 1 = The feedback is automatically chosen within the current sinks CURR1and CURR2 (never DCDC_FB). Only those are used for this selection, which are enabled (currX_mode must not be 00) and not connected to the charge pump (currX_on_cp must be 0).

7.4.2 High Current Sinks CURR30, CURR31, CURR32, CURR33

These current sinks have a preview and strobe setting. The preview and strobe can be controlled by software (register bit) or GPIO2 can be programmed to enter preview mode (polarity programmable) and GPI can be programmed to enter strobe mode (polarity programmable).

In strobe mode, a timeout timer protects the flash leds with a settable timeout of 100ms to 1600ms. This timer has the following modes:

- Flash time defined by timeout timer (Ts) independent of strobe signal (Mode 1)
- Flash time limited to timeout or end of strobe pulse (Mode 2)
- Flash time identical to strobe pulse time (Mode 3)

GPIO1 can be programmed to be used as TXMasking function. This function quickly reduces the current during strobing from strobe levels to preview levels. The timeout counter is not affected by this input.

Figure 16 – Flash Mode 1 – Flash time defined by timeout timer (Ts) independent of strobe signal (Strobe on)

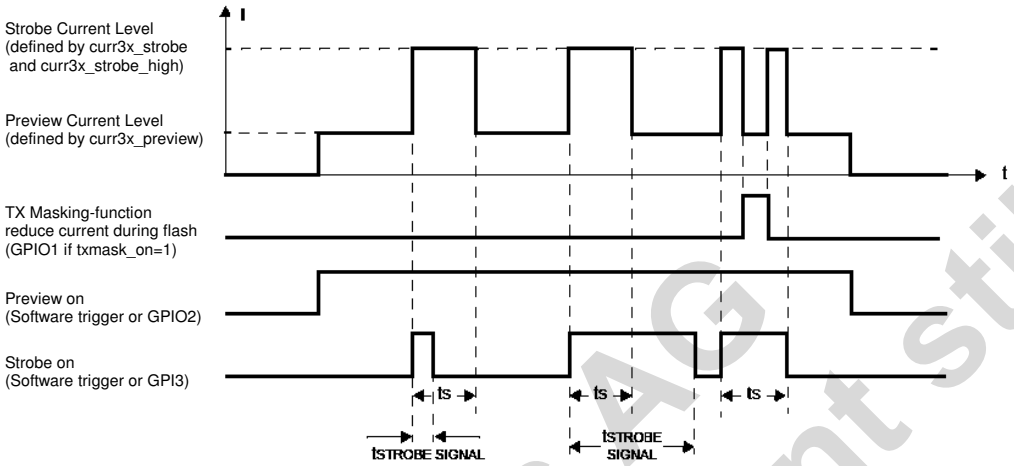


Figure 17 – Flash Mode 2 – Flash time limited to timeout or end of strobe pulse

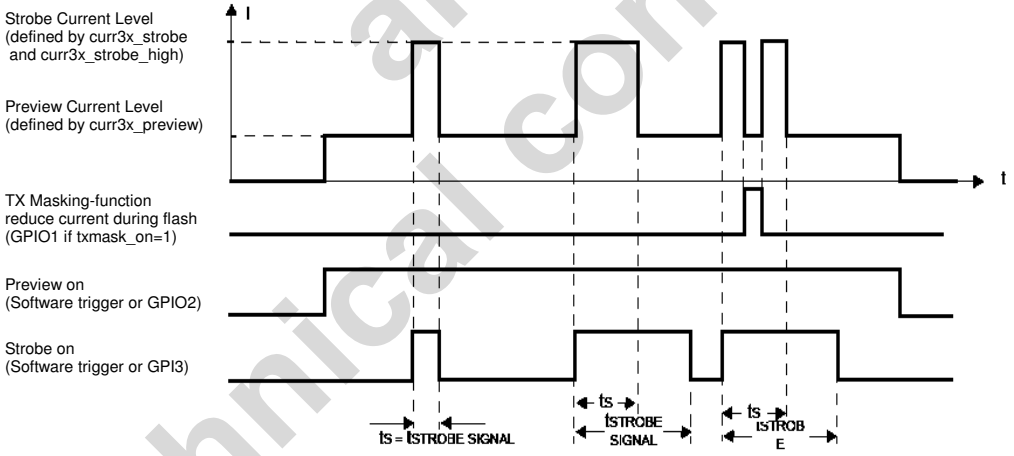


Figure 18 – Flash Mode 3 – Flash time identical to strobe pulse time

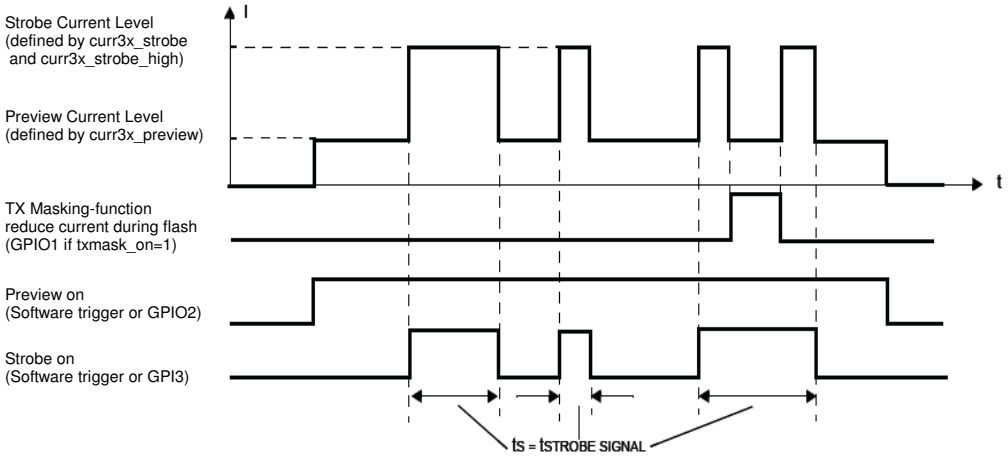


Table 13 – High Current Sinks CURR30,31,32,33 Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{BIT7}	Current sink if Bit7 = 1		76.8		mA	For V(CURRx) > 0.2 / 0.4V
I_{BIT6}	Current sink if Bit6 = 1		38.4			
I_{BIT5}	Current sink if Bit5 = 1		19.2			
I_{BIT4}	Current sink if Bit4 = 1		9.6			
I_{BIT3}	Current sink if Bit3 = 1		4.8			
I_{BIT2}	Current sink if Bit2 = 1		2.4			
I_{BIT1}	Current sink if Bit1 = 1		1.2			
I_{BIT0}	Current sink if Bit0 = 1		0.6			
Δ	absolute Accuracy	-15		+15	%	All Current sinks; V(CURR3x) < VBAT-1.0V
V_{CURR3X}	CURR30,31,32,33 Voltage Compliance Range	0.2		CPOUT	V	0-150mA range
V_{CURR3X_HP}		0.4		CPOUT	V	150mA-300mA range

7.4.2.1 High Current Sinks CURR3x Registers

Addr: 12h		Curr3 control1		
		This register select the modes of the current sinks30..33 current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	preview_off_after strobe	0b	R/W	Select the switch off mode after strobe pulse 0=normal preview/strobe mode, 1=switch off preview after strobe duration has expired To reinitiate the torch mode the preview_ctrl has to be set off and on again
2:1	preview_ctrl	00b	R/W	Preview is triggered by 00b = off 01b = software trigger (setting this bit automatically triggers preview) 10b = GPIO2 active high 11b = GPIO2 active low

Addr: 12h		Curr3 control1		
		This register select the modes of the current sinks30..33 current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
3	txmask_on	0b	R/W	Enables the txmask operation 0b = disabled 1b = During Strobe current is reduced to Preview levels if GPIO1 =1
4	curr3x_ext_ovtemp	0b	R/W	Selects overtemperature switch off of flash LED 0b = normal operation of CURR3x 1b = if the voltage on GPIO2 drops below 1.25V, CURR3x is switched from strobe to preview current levels (can be used to monitor the temperature of the flash led)
5	curr3x_strobe_high	0b	R/W	Doubles curr3x current during strobe 0b = normal operation of CURR3x (0..153 mA) 1b = Doubles current during strobe (0..300mA)
6	txmask_invert	0b	R/W	Inverts the GPIO1 input for txmask function 0b = GPIO1 not inverted 1b = GPIO1 inverted

Addr: 11h		Curr3 strobe control		
		This register select the modes of the current sinks30..33 current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	strobe_ctrl	00b	R/W	Strobe is triggered by 00b = off 01b = software trigger (setting this bit automatically triggers strobe) 10b = GPI active high 11b = GPI active low
3:2	strobe_mode	00b	R/W	Selects strobe mode 00b = Mode 1 (Tstrobe=Ts; strobe trigger signal >= 10µs) 01b = Mode 2 (Tstrobe=max Ts) 10b = Mode 3 (Tstrobe = strobe signal) 11b = not used
7:4	strobe_timing	0000b	R/W	Selects strobe time (Ts) 0000b = 100 msec 0001b = 200 msec 0010b = 300 msec 0011b = 400 msec 0100b = 500 msec 0101b = 600 msec 0110b = 700 msec 0111b = 800 msec 1000b = 900 msec 1001b = 1000 msec 1010b = 1100 msec 1011b = 1200 msec 1100b = 1300 msec 1101b = 1400 msec 1110b = 1500 msec 1111b = 1600 msec

Addr: 0Eh		Curr3x strobe		
		This register select the strobe current of the current sinks30..33		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	curr3x_strobe	00	R/W	Selects strobe current (curr3x_strobe_high can double the current setting) 00h = 0 mA 01h = 0.6mA (1.25mA if curr3x_strobe_high = 1) ... F0h = 150mA (300mA if curr3x_strobe_high = 1) … FFh = 153mA

Note: Do not exceed 300mA for curr3x_strobe.

Addr: 0Fh		Curr3x preview		
		This register select the preview current of the current sinks30..33		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	curr3x_preview	00	R/W	Selects peview current 00h = 0 mA 01h = 0.6mA ... FFh = 153mA

Addr: 10h		Curr3x other		
		This register selects the current of the current sinks30..33		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	curr3x_other	00	R/W	Selects curr3x current, if curr30, curr31, curr32 or curr33 are not used for strobe/preview (CurX_mode=11b) 00h = 0 mA 01h = 0.6mA ... FFh = 153mA

Addr: 03h		curr3 control		
		This register select the mode of the current sinks30 - 33		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	curr30_mode	0	R/W	Select the mode of the current sink curr30 00b = off 01b = strobe/preview 10b = curr3x_other PWM controlled 11b = curr3x_other; do not use softdim_pattern=1
3:2	curr31_mode	0	R/W	Select the mode of the current sink curr31 00b = off 01b = strobe/preview 10b = curr3x_other PWM controlled 11b = curr3x_other; do not use softdim_pattern=1
5:4	curr32_mode	0	R/W	Select the mode of the current sink curr32 00b = off 01b = strobe/preview 10b = curr3x_other PWM controlled 11b = curr3x_other; do not use softdim_pattern=1
7:6	curr33_mode	0	R/W	Select the mode of the current sink curr33 00b = off 01b = strobe/preview 10b = curr3x_other PWM controlled 11b = curr3x_other; do not use softdim_pattern=1

Addr: 18h		Pattern control		
		This register controls the LED pattern		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	pattern_color	0	R/W	Defines the pattern type for the RGBx current sinks 0b = single 32 bit pattern (also set rgbx_mode = 11) 1b = RGB pattern with each 10 bits (set all rgbx_mode = 11)
2:1	pattern_delay	0	R/W	Delay between pattern 00b = 0 sec 01b = 1 sec 10b = 2 sec 11b = 3 sec
3	softdim_pattern	0b	R/W	Enable the 'soft' dimming feature for the pattern generator 0 = Pattern generator directly control current sources 1 = 'Soft Dimming' is performed – see section 'Soft Dimming for pattern'
4	curr30_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR30 controlled according curr30_mode register 1b = CURR30 controlled by LED pattern generator
5	curr31_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR31 controlled according curr31_mode register 1b = CURR31 controlled by LED pattern generator
6	curr32_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR32 controlled according curr32_mode register 1b = CURR32 controlled by LED pattern generator
7	curr33_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR33 controlled according curr33_mode register 1b = CURR33 controlled by LED pattern generator

7.4.3 RGB Current Sinks RGB1, RGB2, RGB3 (VANA2,cpext)

The RGB1,RGB2, RGB3 are pins with different functionality. These pins can act as current sinks or as external chargepump. In addition RGB3 can be programmed as Analog LDO supplied by VBAT3

Figure 19 – RGB pin functionality

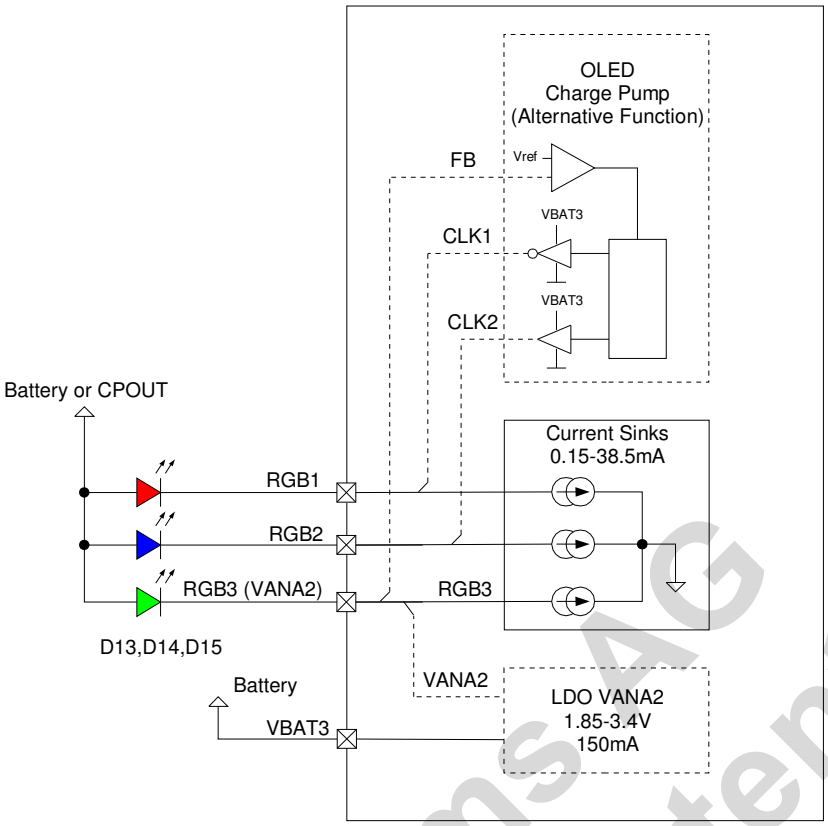


Table 14 – RGB pins Function Overview

Bit settings					Pin Function / Name			Function
rgb1_mode	rgb2_mode	rgb3_mode	cp_ext_on	ldo_ana2_on	RGB1	RGB2	RGB3	
00b	00b	00b	0b	0b	open	open	open	all functions off
01b	01b	01b	0b	0b	RGB1	RGB2	RGB3	Normal current sink operation
10b	10b	10b	0b	0b	RGB1	RGB2	RGB3	PWM current sink operation
xxb	xxb	xxb	1b	xb	CP_CLK1	CP_CLK2	CP_FB	External chargepump operation
xxb	xxb	xxb	0b	1b	open or RGB1	open or RGB2	LDO_ANA2	current sink operation on RGB1 and RGB2, LDO_ANA2 on RGB3 pin

These low voltage current sinks have a resolution of 8 bits. They can be controlled individually by the LED pattern generator (on/off).
External PWM control of these current sinks is also possible and can be enabled by software (Input pin GPIO0).
If the current sink RGB3 (VANA2) is not used, its alternative function is ldo VANA2.

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{BIT7}	Current sink if Bit7 = 1		19.2		mA	For V(CURRx) > 0.2V

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{BIT6}	Current sink if Bit6 = 1		9.6			
I_{BIT5}	Current sink if Bit5 = 1		4.8			
I_{BIT4}	Current sink if Bit4 = 1		2.4			
I_{BIT3}	Current sink if Bit3 = 1		1.2			
I_{BIT2}	Current sink if Bit2 = 1		0.6			
I_{BIT1}	Current sink if Bit1 = 1		0.3			
I_{BIT0}	Current sink if Bit0 = 1		0.15			
Δm	matching Accuracy	-8		+8	%	RGB1,2,3; full scale
Δ	absolute Accuracy	-15		+15	%	V(RGBx) < VBAT-1.0V
RGB1 – RGB3	Voltage compliance	0.2		V(CP OUT)	V	

7.4.3.1 RGB Current Sinks Registers

Addr: 02h		curr rgb control		
		This register select the mode of the current sinks RGB1, RGB2, RGB3		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	rgb1_mode	0	R/W	Select the mode of the current sink RGB1 00b = off 01b = on 10b = PWM controlled 11b = LED pattern controlled
3:2	rgb2_mode	0	R/W	Select the mode of the current sink RGB2 00b = off 01b = on 10b = PWM controlled 11b = LED pattern controlled
5:4	rgb3_mode	0	R/W	Select the mode of the current sink RGB3 00b = off 01b = on 10b = PWM controlled 11b = LED pattern controlled

Addr: 0Bh		Rgb1 current		
		This register controls the RGB current sink current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	rgb1_current	0	R/W	Defines current into Current sink RGB1 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

Addr: 0Ch		Rgb2 current		
		This register controls the RGB current sink current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	rgb2_current	0	R/W	Defines current into Current sink RGB2 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

Addr: 0Dh		Rgb3 current		
		This register controls the RGB current sink current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	rgb3_current	0	R/W	Defines current into Current sink RGB3 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

7.4.4 General Purpose Current Sinks CURR41, CURR42, CURR43

The current sinks CURR42 and CURR43 are only available in the device version AS3688B. In the AS3688B version , the dcdc step up converter is not available.
The general purpose current sink can only be used if the DCDC step up converter is not required. The current sink on the pin DCDC_FB can even be used together with the dcdc converter in current feedback mode without overvoltage protection. These low voltage current sinks have a resolution of 8 bits and can sink up to 40mA.

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{BIT7}	Current sink if Bit7 = 1		19.2		mA	For V(CURRx) > 0.2V
I_{BIT6}	Current sink if Bit6 = 1		9.6			
I_{BIT5}	Current sink if Bit5 = 1		4.8			
I_{BIT4}	Current sink if Bit4 = 1		2.4			
I_{BIT3}	Current sink if Bit3 = 1		1.2			
I_{BIT2}	Current sink if Bit2 = 1		0.6			
I_{BIT1}	Current sink if Bit1 = 1		0.3			
I_{BIT0}	Current sink if Bit0 = 1		0.15			
Δm	matching Accuracy	-8		+8	%	CURR41,42,43; full scale
Δ	absolute Accuracy	-15		+15	%	V(CURR4x) < VBAT-1.0V
Curr41,42,43	Voltage compliance	0.2		VBAT	V	

7.4.4.1 General Purpose Current Sinks CURR41, CURR42, CURR43 Registers

Addr: 04h		curr4 control		
		This register selects the mode of the current sinks CURR41, CURR42, CURR43		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	curr41_mode	0	R/W	Select the mode of the current sink CURR41 00b = off 01b = on 10b = PWM controlled 11b = LED pattern controlled
3:2	curr42_mode	0	R/W	Select the mode of the current sink CURR42 00b = off 01b = on 10b = PWM controlled 11b = LED pattern controlled
5:4	curr43_mode	0	R/W	Select the mode of the current sink CURR43 00b = off 01b = on 10b = PWM controlled 11b = LED pattern controlled

Addr: 13h		Curr41 current		
		This register controls the curr41 current sink current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	curr41_current	0	R/W	Defines current into Current sink CURR41 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

Addr: 14h		Curr42 current		
		This register controls the curr42 current sink current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	curr42_current	0	R/W	Defines current into Current sink CURR42 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

Addr: 15h		Curr43 current		
		This register controls the curr43 current sink current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	curr43_current	0	R/W	Defines current into Current sink CURR43 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

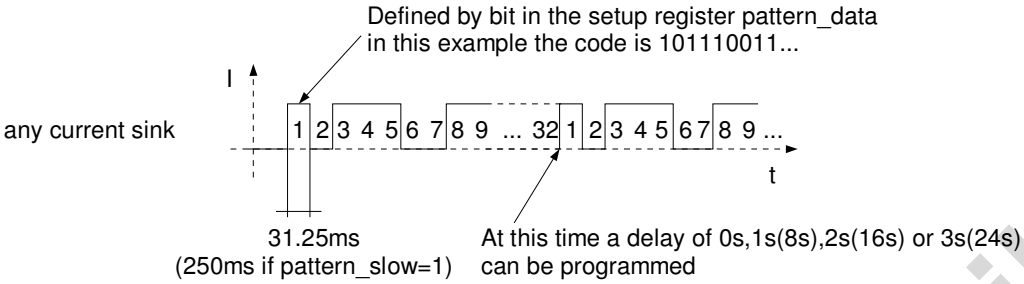
7.4.5 LED Pattern Generator

The LED pattern generator is capable of producing a pattern with 32 bits length and 1 second duration (31.25ms for each bit). The pattern itself can be started every second, every 2nd, 3rd or 4th second.

With this pattern all current sinks can be controlled. The pattern itself switches the configured current sources between 0 and their programmed current.

If everything else is switched off, the current consumption in this mode is IBAT. (excluding current through switched on current source) and the charge pump, if required. The charge pump can be automatically switched on/off depending on the pattern (see register cp_auto_on in the charge pump section) to reduce the overall current consumption.

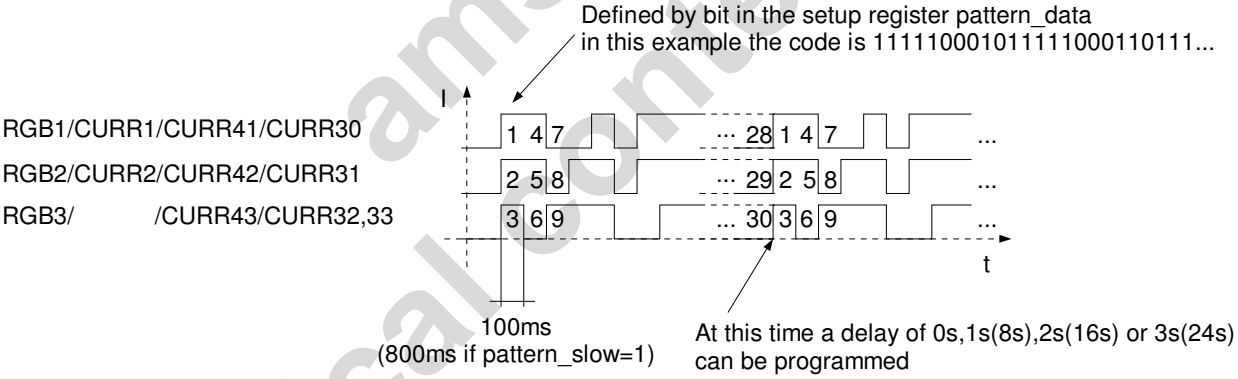
Figure 20 – LED Pattern Generator AS3688 for pattern_color = 0



To select the different current sinks to be controlled by the LED pattern generator, see the 'xxxx'_mode registers (where 'xxxx' stands for the to be controlled current sink, e.g. curr1_mode for CURR1 current sink). See also the descirption of the different current sinks.

To allow the generator of a color patterns set the bit pattern_color to '1'. Then the pattern can be connected e.g. to RGB1/RGB2/RGB3 as follows:

Figure 21 – LED Pattern Generator AS3688 for pattern_color = 1



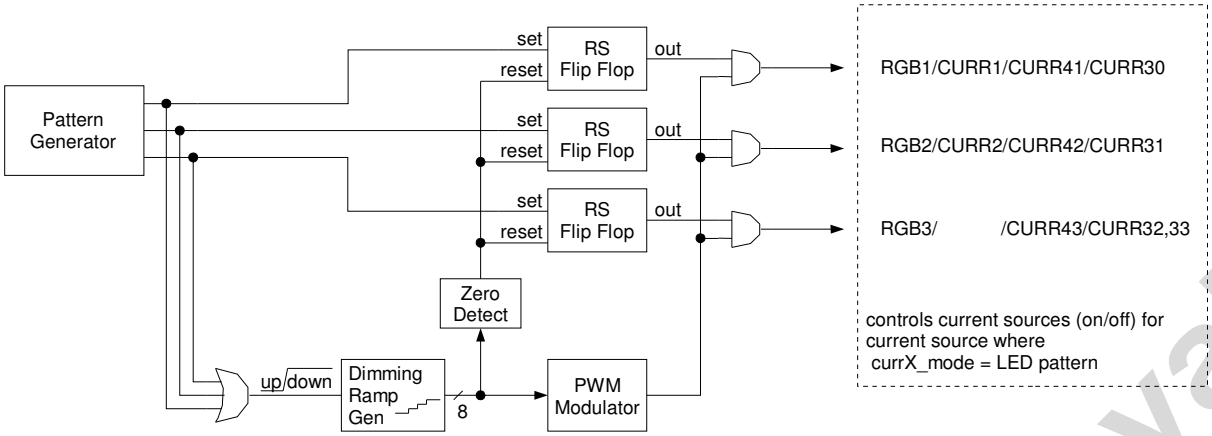
Only those current sinks will be controlled, where the 'xxxx'_mode register is configured for LED pattern.

If the register bit pattern_slow is set, all pattern times are increased by a factor of eigth. (bit duration: 250ms if pattern_color=0 / 800ms if pattern_color=1, delays between pattern up to 24s).

7.4.5.1 Soft Dimming for Pattern

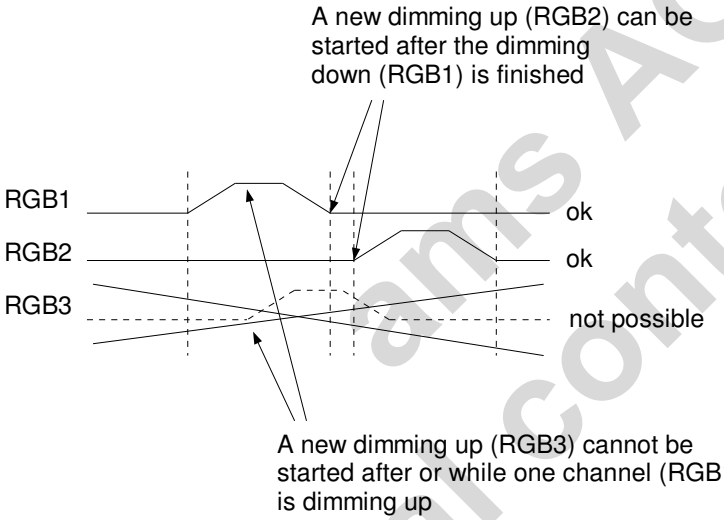
The internal pattern generator can be combined with the internal pwm dimming modulator to obtain as shown in the following figure:

Figure 22 – Softdimming Architecture for the AS3688 (softdim_pattern=1 and pattern_color = 1)



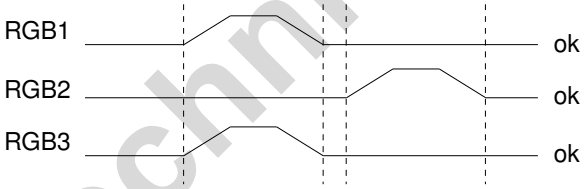
With the AS3688 smooth fade-in and fade-out effects can be automatically generated.
As there is only one dimming ramp generator and one pwm modulator following constraints have to be considered when setting up the pattern (applies only if pattern_color=1):

Figure 23 – Softdimming example Waveform for RGB1, RGB2 and RGB3



However using the identical dimming waveform for two channels is possible as shown in the following figure:

Figure 24 – Softdimming example Waveform for RGB1, RGB2 and RGB3



7.4.5.2 LED Pattern Registers

Addr: 19h,1Ah,1Bh,1Ch		Pattern data0, Pattern data1, Pattern data2, Pattern data3		
		This registers contains the pattern data for the RGB current sinks.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	pattern_data0[7:0] [1]	0	R/W	Pattern data0; if this register is changed and patern_color=1 no current source must have currX_mode = 'LED pattern controlled' (11)
7:0	pattern_data1[15:8] [1]	0	R/W	Pattern data1; if this register is changed and patern_color=1 no current source must have currX_mode = 'LED pattern controlled' (11)
7:0	pattern_data2[23:16] [1]	0	R/W	Pattern data2; if this register is changed and patern_color=1 no current source must have currX_mode = 'LED pattern controlled' (11)
7:0	pattern_data3[31:24] [1]	0	R/W	Pattern data3; if this register is changed and patern_color=1 no current source must have currX_mode = 'LED pattern controlled' (11)

Note:

1. Update any of the pattern register only if none of the current sources is connected to the pattern generator ('xxxx'_mode must not be 11b). The pattern generator is automatically started at the same time when any of the current sources is connected to the pattern generator

Addr: 18h		Pattern control		
		This register controls the LED pattern		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	pattern_color	0	R/W	Defines the pattern type for the current sinks 0b = single 32 bit pattern (also set currX_mode = 'LED pattern controlled (11)) 1b = RGB pattern with each 10 bits (also set currX_mode = 'LED pattern controlled (11))
2:1	pattern_delay	0	R/W	Delay between pattern 00b = 0 sec 01b = 1 sec (8 sec if pattern_slow=1) 10b = 2 sec (16 sec if pattern_slow=1) 11b = 3 sec (24 sec if pattern_slow=1)
3	softdim_pattern	0b	R/W	Enable the 'soft' dimming feature for the pattern generator 0 = Pattern generator directly control current sources 1 = 'Soft Dimming' is performed – see section 'Soft Dimming for pattern'; do not use for CURR1 or CURR2; do not set CURR3x_mode to 'other' if softdim_pattern=1
4	curr30_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR30 controlled according curr30_mode register 1b = CURR30 controlled by LED pattern generator
5	curr31_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR31 controlled according curr31_mode register 1b = CURR31 controlled by LED pattern generator
6	curr32_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR32 controlled according curr32_mode register 1b = CURR32 controlled by LED pattern generator
7	curr33_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR33 controlled according curr33_mode register 1b = CURR33 controlled by LED pattern generator

Addr: 2Ch		gpio_current		
Bit	**Bit Name**	**Default**	**Access**	**Description**
6	pattern_slow	0	R/W	Pattern timing control 0b = normal mode 1b = slow mode (all pattern times are increased by a factor of eight)

7.4.6 Overtemp comparator

If the LED temperature for CURR3x flash led is monitored with an external temperature sensor, the current sink CURR3x can be automatically switched from strobe to preview current levels, if the external temperature sensor's voltage drops below V_{OVtemp}. to avoid overheating of the flash LED.
The overtemperature comparator is multiplexed to GPIO2 and is switched on automatically, if Bit curr3x_ext_ovtemp is set.

Table 15 – Overtemp comparator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{OVtemp}	Comparator switch level	1.22	1.25	1.28	V	

7.4.6.1 Overtemp comparator Registers

Addr: 12h		Curr3 control1		
		This register select the modes of the current sinks30..33 current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	preview_off_after strobe	0b	R/W	Select the switch off mode after strobe pulse 0=normal preview/strobe mode, 1=switch off preview after strobe duration has expired
2:1	preview_ctrl	00b	R/W	Preview is triggered by 00b = off 01b = software trigger 10b = GPIO active high 11b = GPIO active low
3	0	0b	R/W	reserved
4	curr3x_ext_ovtemp	0b	R/W	Selects overtemperature switch off of flash LED 0b = normal operation of CURR3x 1b = if the voltage on GPIO drops below 1.25V (above 1.25V if ext_ov_temp_inv=1), CURR3x is switched from strobe to preview current levels (can be used to monitor the temperature of the flash led or as general input to reduce the current through the flash LED e.g. to temporarily reduce the current from the battery)
5	curr3x_strobe_high	0b	R/W	Doubles curr3x current during strobe 0b = normal operation of CURR3x (0..160 mA) 1b = Doubles current during strobe (0..320mA)
6	0	0b	R/W	reserved
7	curr33_pattern	0b	R/W	Additional CURR33 control bit 0b = CURR33 controlled according curr33_mode register 1b = CURR33 controlled by LED pattern generator

Addr: 2Bh		Curr low voltage status2		
		This register controls the curr42 current sink current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
5	ovtemp_ext	NA	R	Overtemp comparator status bit 0b = no overtemperature, GPIO2>1.25V 1b = overtemperature, GPIO2<1.25V

Addr: 2Ch		gpio current		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	ext_ov_temp_inv	0	R/W	Polarity of external overtemp comparator 0b = active high (Overtemperature when Vgpio>1.25V) 1b = active low (Overtemperature when Vgpio< 1.25V)

7.4.7 External chargepump

This external charge pump uses external schottky diodes and capacitors to generate low current outputs in the range of –15V to +15V. The device delivers a square wave signals and an inverted square wave signals at 250kHz or 500kHz with full Battery voltage swing. Depending on the external configuration the battery voltage is multiplied and / or inverted. A feedback loop with a dedicated regulation pin controls the output voltage by modulating the duty circle.
E.g.: There are 3 Schottky Diodes, 2 Resistors and 3 Capacitors externally required for –6V output voltage.
For the Schottky Diodes the BAS40 (2 diodes in a SOT666 package) is recommended.

Table 16 – External Charge Pump Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
Vfb_{00}	Negative output mode feedback voltage	-20	0	20	mV	Regulated, with internal current source
I_{fb}	Feedback current	9.7	10	10.3	µA	Current sourced at feedback pin for negative mode
Vfb_{01}	Positive output mode feedback voltage	1.22	1.25	1.28	V	Regulated, with two external resistors
$Vout_{00}$	Output Voltage mode 00b		-6		V	with external 600k resistor
$Vout_{01}$	Output Voltage mode 01b		15		V	with external 125kΩ resistor and 1.375 MΩ
η	Efficiency			85	%	Battery Voltage 3.5V
		70				Battery Voltage 4.2V
Iout	Output Current	10			mA	@ -6V
Iout	Output Current	5			mA	@ +15V

7.4.7.1 External chargepump Registers

Addr: 00h		Reg. Control		
		This register enables/disables the LDOs, Charge Pumps, Charge Pump LEDs, current sinks, the Step Up DC/DC Converter.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
4	cp_ext_on	0	R/W	Enable the external chargepump 0b = Disable the external chargepump. 1b = Enable the external chargepump

Addr: 1Dh		Ext. chargepump mode		
		This register selects the modes of the external chargepump		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	cp_ext_mode	0	R/W	Selects the mode of the Ext. charge pump 00b = regulate to negative voltage (e.g.: -6V) 01b = regulate to positive voltage (e.g.:+15V) 10b = unregulated (free running) 11b = reserved Select the mode of the current sink CURR41
3:2	cp_ext_clk<1:0>	0	R/W	Selects the switching frequency 00b = 250kHz 01b = 500kHz 10b = 1MHz 11b = NA
4	cp_ext_lowcurr	0	R/W	Driving capability of ext. charge pump 0b = normal current = Iout 1b = reduced current = Iout / 4 Output noise and ripple will be reduced

7.4.8 PWM Generator

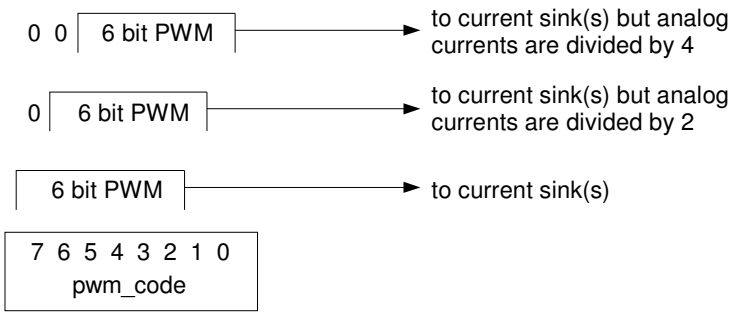
The PWM generator can be used for any current sink (CURR1, CURR2, CURR3x, CURR4x, RGB).. It can be programmed to use the pin GPIO0 (pwm_mode=0) or an internal PWM generator (pwm_mode=1). The setting applies for all current sinks, which are controlled by the pwm generator (e.g. CURR1 is pwm controlled if curr1_mode = 10, RGB1 is pwm controlled if rgb1_mode = 10). The pwm modulated signal (internal / external) can switch on/off the current sinks and therefore depending on its duty cycle change the brightness of an attached LED.

7.4.8.1 Internal PWM Generator

The internal PWM generator uses the 2MHz internal clock as input frequency and its dimming range is 6 bits digital (2MHz / 2^6 = 31.3kHz pwm frequency) and 2 bits analog. Depending on the actual code in the register 'pwm_code' the following algorithm is used:

- If pwm_code bit 7 = 1
  Then the upper 6 bits (Bits 7:2) of pwm_code are used for the 6 bits PWM generation, which controls the selected currents sinks directly
- If pwm_code bit 7 =0 and bit 6 = 1
  Then bits 6:1 of pwm_code are used for the 6 bits PWM generation. This signal controls the selected current sinks, but the analog current of these sinks is divided by 2
- If pwm_code bit 7 and bit 6 = 0
  Then bits 5:0 of pwm_code are used for the 6 bits PWM generation. This signal controls the selected current sinks, but the analog current of these sinks is divided by 4

Figure 25 – PWM Control

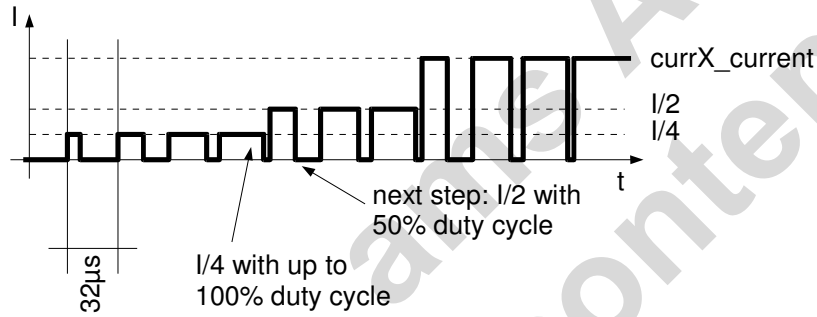


Automatic Up/Down Dimming

If the register pwm_dim_mode is set to 01 (up dimming) or 10 (down dimming) the value within the register pwm_code is increased (up dimming) or decreased (down dimming) every time and amount (either 1/4th or 1/8th) defined by the register pwm_dim_speed. The maximum value of 255 (completely on) and the minimum value of 0 (off) is never exceeded. It is used to smoothly and automatically dim the brightness of the LEDs connceted to any of the current sinks. The PWM code is readable all the time (Also during up and down dimming)

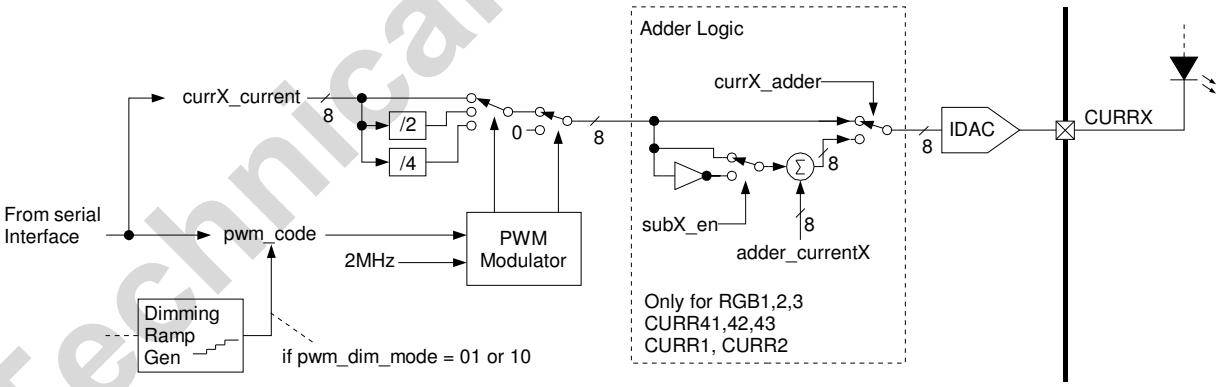
The waveform for up dimming looks as follows (cycles omitted for simplicity):

Figure 26 – PWM Dimming Waveform for up dimming (pwm_dim_mode = 01); currX_mode = PWM controlled (not all steps shown)



The internal pwm modulator circuit controls the current sinks as shown in the following figure:

Figure 27 – PWM Control Circuit (currX_mode = 10b (PWM controlled)); X = any current sink



The adder logic (available for RGB1, RGB2, RGB3, CURR41, CURR42, CURR43, CURR1 and CURR2) is intended to allow dimming not only from 0% to 100% (or 100% to 0%) of currX_current, but also e.g. from 10% to 110% (or 110% to 10%) of currX_current. That means for up dimming the starting current is defined by 0 + currX_adder and the end current is defined by currX_current + currX_adder.
An overflow of the internal bus (8 Bits wide to the IDAC) has to be avoided by the register settings (currX_current + currX_adder must not exceed 255).

If the register subX_en is set, the result from the pwm_modulator is inverted logically. That means for up dimming the starting current is defined by currX_adder - 1 and the end current is defined by currX_adder - currX_current - 1. An overflow of the internal bus (8 Bits wide to the IDAC) has to be avoided by the register settings (currX_adder - currX_current - 1 must not be below zero).
Its purpose is to dim one channel e.g. CURR41 from e.g. 110% to 10% of curr41_current and at the same time dim another channel e.g. CURR42 from 20% to 120% of curr42_current.

Note:

1. The adder logic operates independent of the currX_mode setting, but its main purpose is to work together with the pwm modulator (improved up/down dimming)
2. If the adder logic is not used anymore, set the bit currX_adder to 0. (Setting adder_currentX to 0 is not sufficient)

Figure 28 – PWM Table

	Decrease by 1/4th every step		Decrease by 1/8th every step		Seconds	Seconds	Seconds	Seconds
Step	%Dimming	PWM	%Dimming	PWM	50msec/ Step	25msec/ Step	5msec/ Step	2,5msec/ Step
1	100,0	255	100,0	255	0,00s	0,00s	0,000s	0,000s
2	75,3	192	87,8	224	0,05s	0,03s	0,005s	0,003s
3	56,5	144	76,9	196	0,10s	0,05s	0,010s	0,005s
4	42,4	108	67,5	172	0,15s	0,08s	0,015s	0,008s
5	31,8	81	59,2	151	0,20s	0,10s	0,020s	0,010s
6	23,9	61	52,2	133	0,25s	0,13s	0,025s	0,013s
7	18,0	46	45,9	117	0,30s	0,15s	0,030s	0,015s
8	13,7	35	40,4	103	0,35s	0,18s	0,035s	0,018s
9	10,6	27	35,7	91	0,40s	0,20s	0,040s	0,020s
10	8,2	21	31,4	80	0,45s	0,23s	0,045s	0,023s
11	6,3	16	27,5	70	0,50s	0,25s	0,050s	0,025s
12	4,7	12	24,3	62	0,55s	0,28s	0,055s	0,028s
13	3,5	9	21,6	55	0,60s	0,30s	0,060s	0,030s
14	2,7	7	19,2	49	0,65s	0,33s	0,065s	0,033s
15	2,4	6	16,9	43	0,70s	0,35s	0,070s	0,035s
16	2,0	5	14,9	38	0,75s	0,38s	0,075s	0,038s
17	1,6	4	13,3	34	0,80s	0,40s	0,080s	0,040s
18	1,2	3	11,8	30	0,85s	0,43s	0,085s	0,043s
19	0,8	2	10,6	27	0,90s	0,45s	0,090s	0,045s
20	0,4	1	9,4	24	0,95s	0,48s	0,095s	0,048s
21	**0,0**	**0**	8,2	21	**1,00s**	**0,50s**	**0,100s**	**0,050s**
22			7,5	19	1,05s	0,53s	0,105s	0,053s
23			6,7	17	1,10s	0,55s	0,110s	0,055s
24			5,9	15	1,15s	0,58s	0,115s	0,058s
25			5,5	14	1,20s	0,60s	0,120s	0,060s
26			5,1	13	1,25s	0,63s	0,125s	0,063s
27			4,7	12	1,30s	0,65s	0,130s	0,065s
28			4,3	11	1,35s	0,68s	0,135s	0,068s
29			3,9	10	1,40s	0,70s	0,140s	0,070s
30			3,5	9	1,45s	0,73s	0,145s	0,073s
31			3,1	8	1,50s	0,75s	0,150s	0,075s
32			2,7	7	1,55s	0,78s	0,155s	0,078s
33			2,4	6	1,60s	0,80s	0,160s	0,080s
34			2,0	5	1,65s	0,83s	0,165s	0,083s
35			1,6	4	1,70s	0,85s	0,170s	0,085s

	Decrease by 1/4th every step		Decrease by 1/8th every step		Seconds	Seconds	Seconds	Seconds
Step	%Dimming	PWM	%Dimming	PWM	50msec/ Step	25msec/ Step	5msec/ Step	2,5msec/ Step
36			1,2	3	1,75s	0,88s	0,175s	0,088s
37			0,8	2	1,80s	0,90s	0,180s	0,090s
38			0,4	1	1,85s	0,93s	0,185s	0,093s
39			**0,0**	**0**	**1,90s**	**0,95s**	**0,190s**	**0,095s**

7.4.8.2 PWM Generator Registers

Addr: 16h		**Pwm control**		
		This register controls PWM generator		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	pwm_mode	1b	R/W	Selects the PWM source 0b = Use external PWM from GPIO0 or GPIO2 (defined by pwm_gpio2) 1b = Use internal PWM (default)
2:1	pwm_dim_mode	00b	R/W	Selects the dimming mode 00b = no dimming; actual content of register pwm_code is used for pwm generator 01b = logarithmic up dimming (codes are increased). Start value is actual pwm_code 10b = logarithmic down dimming (codes are decreased) Start value is actual pwm_code; switch off the dimmed current source after dimming is finished to avoid unnecessary quiescent current 11b = NA
5:3	pwm_dim_speed	000b	R/W	Defines dimming speed by increase/descrease pwm_code … 000b = … by 1/4th every 50 msec (total dim time 1.0s) 001b = … by 1/8th every 50 msec (total dim time 1.9s) 010b = … by 1/4th every 25 msec (total dim time 0.5s) 011b = … by 1/8th every 25 msec (total dim time 0.95s) 100b = … by 1/4th every 5 msec (total dim time 100ms) 101b = … by 1/8th every 5 msec (total dim time 190ms) 110b = … by 1/4th every 2.5 msec (total dim time 50ms) 111b = … by 1/8th every 2.5 msec (total dim time 95ms)
6	pwm_gpio2	0b	R/W	Selects the PWM source 0b = Use GPIO0 for external pwm 1b = Use GPIO2 for external pwm

Addr: 17h		**Pwm code**		
		This register controls the Pwm code.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	pwm_code	00b	R/W	Selects the PWM code 00h = Always 0 ... FFh = Always 1

Addr: 30h		Adder Current 1		
		This register defines the current which can be added to CURR1, CURR41, RGB1		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	adder_current1	00b	R/W	Selects the added current value – do not exceed together with currX_current the internal 8 Bit range (see text) 00h = 0 (represents 0mA) ... FFh = 255 (represents 38.25mA)

Addr: 31h		Adder Current 2		
		This register defines the current which can be added to CURR2, CURR42, RGB2		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	adder_current2	00b	R/W	Selects the added current value – do not exceed together with currX_current the internal 8 Bit range (see text) 00h = 0 (represents 0mA) ... FFh = 255 (represents 38.25mA)

Addr: 32h		Adder Current 3		
		This register defines the current which can be added to CURR43, RGB3		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	adder_current3	00b	R/W	Selects the added current value – do not exceed together with currX_current the internal 8 Bit range (see text) 00h = 0 (represents 0mA) ... FFh = 255 (represents 38.25mA)

Addr: 33h		Adder Enable 1		
		Enables the adder circuit for the selected current sources		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	rgb1_adder	0	R/W	Enables adder circuit for current source RGB1 0 = Normal Operation of the current source 1 = adder_current1 gets added to the current source current
1	rgb2_adder	0	R/W	Enables adder circuit for current source RGB2 0 = Normal Operation of the current source 1 = adder_current2 gets added to the current source current
2	rgb3_adder	0	R/W	Enables adder circuit for current source RGB3 0 = Normal Operation of the current source 1 = adder_current3 gets added to the current source current
3	curr41_adder	0	R/W	Enables adder circuit for current source CURR41 0 = Normal Operation of the current source 1 = adder_current1 gets added to the current source current
4	curr42_adder	0	R/W	Enables adder circuit for current source CURR42 0 = Normal Operation of the current source 1 = adder_current2 gets added to the current source current
5	curr43_adder	0	R/W	Enables adder circuit for current source CURR43 0 = Normal Operation of the current source 1 = adder_current3 gets added to the current source current

Addr: 34h		Adder Enable 2		
		Enables the adder circuit for the selected current sources		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr1_adder	0	R/W	Enables adder circuit for current source CURR1 0 = Normal Operation of the current source 1 = adder_current1 gets added to the current source current
1	curr2_adder	0	R/W	Enables adder circuit for current source CURR2 0 = Normal Operation of the current source 1 = adder_current2 gets added to the current source current

Addr: 35h		Subtract Enable		
		Enable the inversion from the signal from the pwm generator		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	sub_en1	0	R/W	Inverts the signal from the pwm generator 0 = Direct Operation (no inversion) 1 = The signal from the pwm generator for which the adder is enabled (curr1_adder = 1, curr41_adder = 1, rgb1_adder = 1) is inverted
1	sub_en2	0	R/W	Inverts the signal from the pwm generator 0 = Direct Operation (no inversion) 1 = The signal from the pwm generator for which the adder is enabled (curr2_adder = 1, curr42_adder = 1, rgb2_adder = 1) is inverted
2	sub_en3	0	R/W	Inverts the signal from the pwm generator 0 = Direct Operation (no inversion) 1 = The signal from the pwm generator for which the adder is enabled (curr42_adder = 1, rgb3_adder = 1) is inverted

7.5 General Purpose Input / Outputs

GPIO0 :GPIO2, GPI are four highly-configurable general purpose input/output pins which can be used for the following functionality (each GPIO pin is independent from the other GPIO pins):

- Digital Schmitt-Trigger Input
- Digital Output with 4mA Driving Capability at 2.8V Supply (VDD_GPIO)
- Tristate Output
- Analog Input to the ADC (GPIO0, GPIO1, GPIO2, GPI)
- Strobe for Camera Flash Current Sink (GPI)
- Preview Current set input for Camera Flash Current Sink (GPIO2)
- PWM operation with all current sinks (GPIO0); number of current sources using this PWM input is fully configurable
- Flash led overtemperature protection (GPIO2)
- Default Mode for GPI is Input

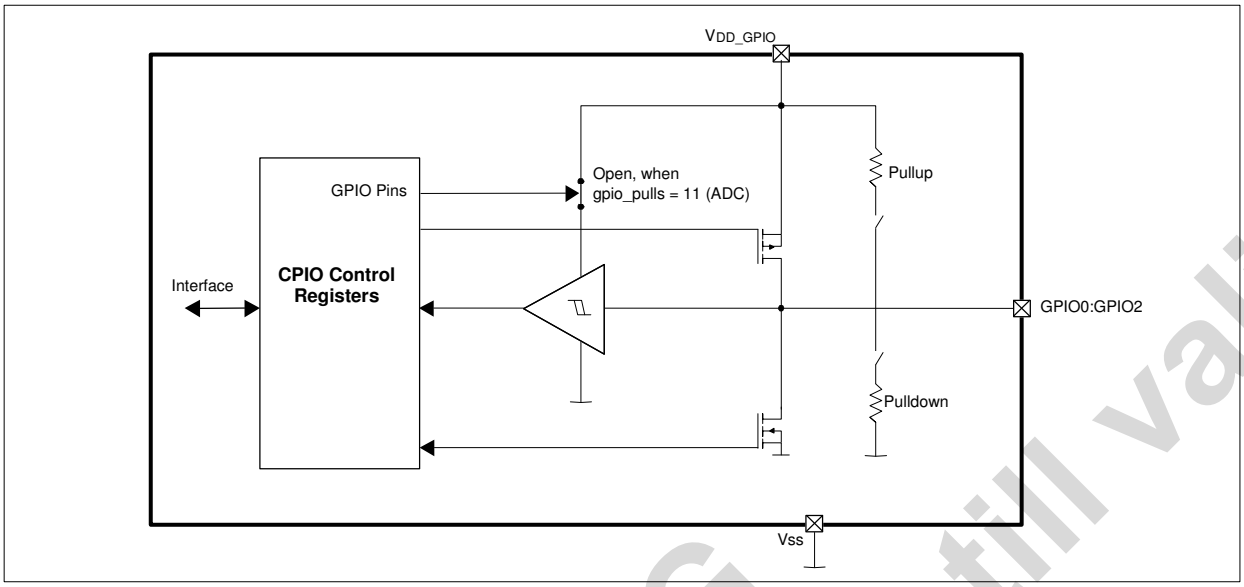
  Default Mode for GPIO0, GPIO1 and GPIO2 is Input (Pull-Down)

  GPIO4 not applicable in the AS3688

Table 17 – GPIO Pin Function Summary

GPIO Pin	Pin #	Configuration	Additional Function
GPIO0	TBD	Digital Input, Totem-Pole Output (Push/Pull), Open Drain (PMOS or NMOS), High-Z, Pull-Down or Pull-Up Resistor	ADC Input; PWM Input
GPIO1	TBD		ADC Input; TXMask input
GPIO2	TBD		ADC Input; Preview Input for Photocamera Flash LED (CURR3*x*); PWM Input
GPI	TBD	Digital Input	ADC Input; Strobe Input for Photocamera Flash LED (CURR3*x*)

Figure 29 – GPIO Pin Connections



7.5.1 GPIO Characteristics

Table 18 – GPIO DC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
Rpull	Pull up/Pull down Resistance	30	75	kΩ	
Vgpio	Supply Voltage	1.5	3.3	V	
VIH	High Level Input Voltage	0.7·Vgpio		V	
VIL	Low Level Input Voltage		0.3· Vgpio	V	
VHYS	Hysteresis	0.1· Vgpio		V	
ILEAK	Input Leakage Current	-5	5	µ A	To Vgpio and VSS
VOH	High Level Output Voltage	0.8·Vgpio		V	at - Iout
VOL	Low Level Output Voltage		0.2· Vgpio	V	at Iout
Iout	Driving Capability	4		mA	Vgpio = 2.8V, **gpioX_low_curr** = 1 (page gpio0_low_curr)
		16			Vgpio = 2.8V, **gpioX_low_curr** = 0
		1			Vgpio = 1.5V, **gpioX_low_curr** = 0 guaranteed by design.
		4			Vgpio = 1.5V, **gpioX_low_curr** = 1 guaranteed by design.
CLOAD	Capacitive Load		50	pF	

Vgpio is used as the supply voltage for all GPIOs.

7.5.2 GPIO Registers

Addr: 05h		GPIO Output		
		This register controls GPIO outputs.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	gpio0_out	0	R/W	Writes a logic signal to pin GPIO0; this is independent of any other bit setting e.g., gpio0_mode.
1	gpio1_out	0	R/W	Writes a logic signal to pin GPIO1; this is independent of any other bit setting e.g., gpio1_mode.
2	gpio2_out	0	R/W	Writes a logic signal to pin GPIO2; this is independent of any other bit setting e.g., gpio2_mode.
3	gpi_en	0	R/W	Enables the GPI input. Set to 1 if used for strobe trigger. 0 = input disabled 1 = input enabled; can be used for strobe trigger
4	gpi_curr30_en	0	R/W	Enables the CURR30 input. 0 = input disabled 1 = input enabled
5	gpi_curr31_en	0	R/W	Enables the CURR31 input. 0 = input disabled 1 = input enabled
6	gpi_curr32_en	0	R/W	Enables the CURR32 input. 0 = input disabled 1 = input enabled
7	gpi_curr33_en	0	R/W	Enables the CURR33 input. 0 = input disabled 1 = input enabled

Addr: 06h		GPIO Signal		
		This register controls GPIO outputs.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	gpio0_in	N/A	R	Reads a logic signal from pin GPIO0; this is independent of any other setting e.g., bits gpio1_mode.
1	gpio1_in	N/A	R	Reads a logic signal from pin GPIO1; this is independent of any other setting e.g., bits gpio1_mode.
2	gpio2_in	N/A	R	Reads a logic signal from pin GPIO2; this is independent of any other setting e.g., bits gpio1_mode.
3	gpi_in	N/A	R	Reads a logic signal from pin GPI; if gpi_en=1
4	curr30_in	N/A	R	Reads a logic signal from pin CURR30; if gpi_curr30_en=1
5	curr31_in	N/A	R	Reads a logic signal from pin CURR31; if gpi_curr31_en=1
6	curr32_in	N/A	R	Reads a logic signal from pin CURR32; if gpi_curr32_en=1
7	curr33_in	N/A	R	Reads a logic signal from pin CURR33; if gpi_curr33_en=1

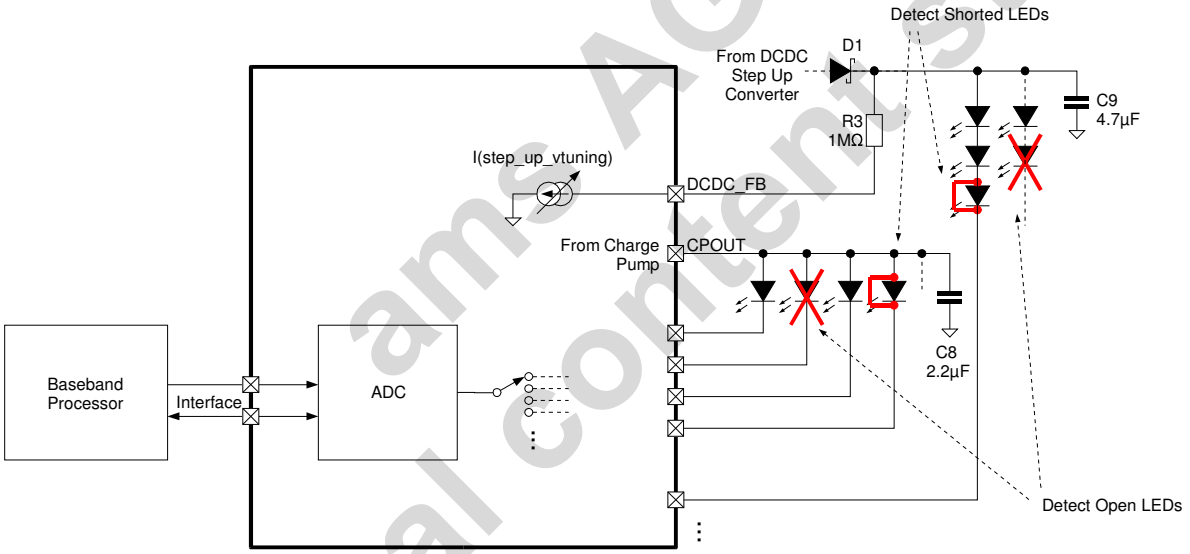
Addr: 1Eh		GPIO01_control		
		This register controls GPIO0 and GPIO1 pin functions.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	gpio0_mode	00	R/W	Defines the direction for pin GPIO0. 00 = Input only or used for PWM 01 = Output (push and pull). 10 = Output (open drain, only push; only NMOS is active). 11= Output (open drain, only pull; only PMOS is active).
3:2	gpio0_pulls	01	R/W	Adds the following pullup/pulldown to pin GPIO0; this is independent of setting of bits gpio0_mode. 00 = None 01 = Pulldown 10 = Pullup 11= ADC input (gpio0_mode = XX); recommended for analog signals.
5:4	gpio1_mode	00	R/W	Defines the direction for pin GPIO1. 00 = Input only; can be used for TXMask 01 = Output (push and pull). 10 = Output (open drain, only push; only NMOS is active). 11= Output (open drain, only pull; only PMOS is active).
7:6	gpio1_pulls	01	R/W	Adds the following pullup/pulldown to pin GPIO1; this is independent of setting of bits gpio1_mode. 00 = None 01 = Pulldown 10 = Pullup 11= ADC input (gpio1_mode = XX); recommended for analog signals.

Addr: 1Fh		GPIO23 control		
		This register controls pins GPIO2 pin functions.		
Bit	**Bit Name**	**Default**	**Access**	**Description.**
1:0	gpio2_mode	00	R/W	Defines the direction for pin GPIO2. 00 = Input only; can be used for PWM or preview mode 01 = Output (push and pull). 10 = Output (open drain, only push; only NMOS is active). 11= Output (open drain, only pull; only PMOS is active).
3:2	gpio2_pulls	11	R/W	Adds the following pullup/pulldown to pin GPIO2; this is independent of setting of bits gpio2_mode. 00 = None 01 = Pulldown 10 = Pullup 11= ADC input (gpio2_mode = XX); recommended for analog signals.
7:4				N/A

Addr: 20h		GPIO driving cap		
		This register enables low current mode for GPIOs.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	gpio0_low_curr	0	R/W	Defines the driving capability of pin GPIO0. 0 = Iout 1 = Iout /4
1	gpio1_low_curr	0	R/W	Defines the driving capability of pin GPIO1. 0 = Iout 1 = Iout /4
2	gpio2_low_curr	0	R/W	Defines the driving capability of pin GPIO2. 0 = Iout 1 = Iout /4
7:3				N/A

7.6 LED Test

Figure 30 – LED Function Testing



The AS3688 supports the verification of the functionality of the connected LEDs (open and shorted LEDs can be detected). This feature is especially useful in production test to verify the correct assembly of the LEDs, all its connectors and cables. It can also be used in the field to verify if any of the LEDs is damaged. A damaged LED can then be disabled (to avoid unnecessary currents).
The current sources, charge pump, dcdc converter and the internal ADC are used to verify the forward voltage of the LEDs. If this forward voltage is within the specified limits of the LEDs, the external circuitry is assumed to operate.

7.6.1 Function Testing for single LEDs connected to the Charge Pump

For any current source connected to the charge pump (usually RGB{1,2,3}, CURR{30,31,32,33,41,42,43}) where only one LED is connected between the charge pump and the current sink (see Figure 1) use:

Table 19 – Function Testing for LEDs connected to the Charge Pump

Step	Action	Example Code
1.	Switch on the charge pump and set it into manual 1:2 mode (to avoid automatic mode switching during measurements)	Reg 23h <- 14h (cp_mode = 1:2, manual) Reg 00h <- 04h (cp _on = 1)

Table 19 – Function Testing for LEDs connected to the Charge Pump

Step	Action	Example Code
2.	Switch on the current sink for the LED to be tested	e.g. for register CURR31set to 9mA use Reg 10h <- 0Fh (curr3x_other = 9mA) Reg 03h <- 0ch (curr31_mode = curr3x_other)
3.	Measure with the ADC the voltage on CP_OUT	Reg 26h <- 95h (adc_select=CP_OUT,start ADC) Fetch the ADC result from Reg 27h and 28h
4.	Measure with the ADC the voltage on the switched on current sink	Reg 26h <- 8bh (adc_select=CURR31,start ADC) Fetch the ADC result from Reg 27h and 28h
5.	Switch off the current sink for the LED to be tested	Reg 03h <- 00h (curr31_mode = off)
6.	Compare the difference between the ADC measurements (which is the actual voltage across the tested LED) against the specification limits of the tested LED	Calculation performed in baseband uProcessor
7.	Do the same procedure for the next LED starting from point 2	Jump to 2. If not all the LEDs have been tested
8.	Switch off the charge pump set chargepump automatic mode	Reg 00h <- 00h (cp _on = 0) Reg 23h <- 00h

Note: For CURR41,42,43 first set the charge pump into 1:1 mode and test if the LED is shorted. Then use the above described procedure.

7.6.2 Function Testing for LEDs connected to the Step Up DCDC Converter

For LEDs connected to the DCDC converter (usually current sinks CURR1and CURR2) use the following procedure:

Table 20 – Function Testing for LEDs connected to the DCDC converter

Step	Action	Example Code
1.	Switch on the current sink for the LED string to be tested (CURR1 or CURR2)	e.g. Test LEDs on CURR1: Reg 01h <- 01h (curr1_mode=on) Reg 09h <- 3ch (curr1 = 9mA)
2.	Select the feedback path for the LED string to be tested (e.g. step_up_fb = 01 for LED string on CURR1)	Reg 21h <- 02h (feedback=curr1)
3.	Set the current for step_up_vtuning exactly above the maximum forward voltage of the tested LED string + 0.6V (for the current sink) + 0.25V; add 6% margin (accuracy of step_up_vtuning); this sets the maximum output voltage limit for the DCDC converter	e.g. 4 LEDs with UfMAX = 4.1V gives 17.25V +6% = 18.29V; if R3=1MΩ and R4 = open, then select step_up_vtuning = 18 (Reg 21h <- 92h; results in 19.25V overvoltage protection voltage – see table in DCDC section)
4.	Set stepup_prot = 1	Reg 22h <- 04h
5.	Switch on the DCDC converter	Reg 00h <- 08h
6.	Wait 1ms (DCDC startup time)	
7.	Measure the voltage on DCDC_FB (ADC)	Reg 26h <- 96h (adc_select=DCDC_FB, start ADC; Fetch the ADC result from Reg 27h and 28h)
8.	If the voltage on DCDC_FB is above 1.0V, the tested LED string is broken – then skip the following steps	(Code >199h)
9.	Switch off the overvoltage protection (stepup_prot = 0)	Reg 22h <- 00h
10.	Reduce step_up_vtuning step by step until the measured voltage on DCDC_FB (ADC) is above 1.0V.	e.g.: Reg 21h <- 62h (step_up_vtuning=12): ADC result=1,602V
11.	Measure voltage on DCDC_FB	e.g. DCDC_FB=1.602V
12.	Switch off the DCDC converter	Reg 00h <- 00h

Table 20 – Function Testing for LEDs connected to the DCDC converter

Step	Action	Example Code
13.	The voltage on the LED string can be calculated now as follows (R4 = open): $VLED_{STRING}$ = V(DCDC_FB) + I(step_up_vtuning) * R3 – 0.5V (current sinks feedback voltage: VFB2). V(DCDC_FB) = ADC Measurement from point 11 I(step_up_vtuing) = last setting used for point 10	e.g.: VLED = (1.602V + 12V – 0.5V) / 4 = 3.276V
14.	Compare the calculated value against the specification limits of the tested LEDs	

With the above described procedures electrically open and shorted LEDs can be automatically detected. To reduce the settling time of the DCDC converter to changes of step_up_vtuning, the external capacitors C_{10} and C_{11} can be changed to C_{10}=150pF and C_{11}=1.5nF.

7.7 Analog-To-Digital Converter

The AS3688 has a built-in 10-bit successive approximation analog-to-digital converter (ADC). It is internally supplied by V2_5, which is also the full-scale input range (0V defines the ADC zero-code). For input signal exceeding V2_5 (typ. 2.5V) a resistor divider with a gain of 0.4 ($Ratio_{prescaler}$) is used to scale the input of the ADC converter. Consequently the resolution is:

Table 21 – ADC Input Ranges, Compliances and Resolution

Channels (Pins)	Input Range	V_{LSB}	Note
GPIO0, GPIO1, GPIO2, GPI, DCDC_FB	0V-2.5V	2.44mV	V_{LSB}=2.5/1024
ADC_{TEMP_CODE}	TBD	1 / ADC_{TC}	junction temperature
RGB1,RGB2,RGB3, CURR{30, 31, 32, 33, 41, 42, 43} VBAT2, CP_OUT	0V-5.5V	6.1mV	V_{LSB}=2.5/1024 * 1/0.4; internal resistor divider used
CURR1, CURR2	0V-1.0V	2.44mV	V_{LSB}=2.5/1024

Table 22 – ADC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Resolution	10			Bit	
Vin	Input Voltage Range	VSS		Vsupply	V	Vsupply = V2_5
D_{NL}	Differential Non-Linearity		± 0.25		LSB	
I_{NL}	Integral Non-Linearity		± 0.5		LSB	
Vos	Input Offset Voltage		± 0.25		LSB	
Rin	Input Impedance	100			MΩ	
Cin	Input Capacitance			9	pF	
Vsupply (V2_5)	Power Supply Range		2.5		V	± 2%, internally trimmed used as reference for ADC converter
Idd	Power Supply Current		500		µ A	During conversion only.
Idd	Power Down Current		100		nA	
T_{TOL}	Temperature Sensor Accuracy		+/-5		°C	@ 25 °C
$ADC_{TOFFSET}$	ADC temperature measurement offset value		375		Code	

Table 22 – ADC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
ADCTC	Code temperature coefficient		1.2939		Code/°C	Temperature change per ADC LSB
Ratioprescaler	Ratio of Prescaler		0.4			For all low voltage current sinks, CP_OUT and VBAT2
VGPIOCURR	Voltage Compliance of current source for GPIO	0.0		1.35	V	Current Source for pin GPIO2
IGPIOCURR	Current Accuracy for GPIO current source	-1.0µA	1-15µA	+1.0µA	V	
Transient Parameters (2.5V, 25 ºC)						
Tc	Conversion Time		27		µ s	All signal are Internally generated and triggered by start_conversion
fc	Clock Frequency		1.0		MHz	
ts	Settling Time of S&H		4		µ s	

The junction temperature (TJUNCTION) can be calculated with the following formula (ADCTEMP_CODE is the adc conversion result for channel 15 selected by register adc_select = 000100b):

$$T_{JUNCTION}\,[°C] = ADC_{TOFFSET} - ADC_{TC} * ADC_{TEMP\_CODE}$$

7.7.1 ADC Registers

Addr: 26h		ADC_control		
		This register input source selection and initialization of ADC.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
5:0	adc_select[1]	0	R/W	Selects input source as ADC input. 000000 (00h) = GPIO0 000001 (01h) = GPIO1 000010 (02h) = GPIO2 000011 (03h) = GPI 000100 (04h) = reserved 000101 (05h) = RGB1 000110 (06h) = RGB2 000111 (07h) = RGB3 001000 (08h) = CURR1 001001 (09h) = CURR2 001010 (0Ah) = CURR30 001011 (0Bh) = CURR31 001100 (0Ch) = CURR32 001101 (0Dh) = CURR33 001110 (0Eh) = CURR41 001111 (0Fh) = CURR42 010000 (10h) = CURR43 010001 (11h) = reserved 010010 (12h) = reserved 010011 (13h) = reserved 010100 (14h) = VBAT2 010101 (15h) = CP_OUT 010110 (16h) = DCDC_FB 010111 (17h) = ADCTEMP_CODE (junction temperature) 011xxx, 1xxxxx = reserved
6				NA
7	start_conversion	N/A	W	Writing a 1 into this bit starts one ADC conversion cycle.

Notes:

1. See Table 'ADC Input Ranges, Compliances and Resolution' for ADC ranges and possible

Addr: 2Ch		GPIO current		
		controls the output current of pin GPIO (e.g. for light sensor)		
Bit	**Bit Name**	**Default**	**Access**	**Description**
3:1	gpio2_curr	000	R/W	000 off 001 2uA 010 4uA … 111 14uA

Addr: 27h		ADC_MSB Result		
		Together with Register 27h, this register contains the results (MSB) of an ADC cycle.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
6:0	D9:D3	N/A	R	ADC results register.
7	result_not_ready	N/A	R	Indicates end of ADC conversion cycle. 0 = Result is ready. 1 = Conversion is running.

Addr: 28h		ADC_LSB Result		
		Together with Register 28h, this register contains the results (LSB) of an ADC cycle		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2:0	D2:D0	N/A	R	ADC result register.
7:3				N/A

Figure 31 – ADC Timing Diagrams (TBD: TODO: Increase Sample Time to 16us)

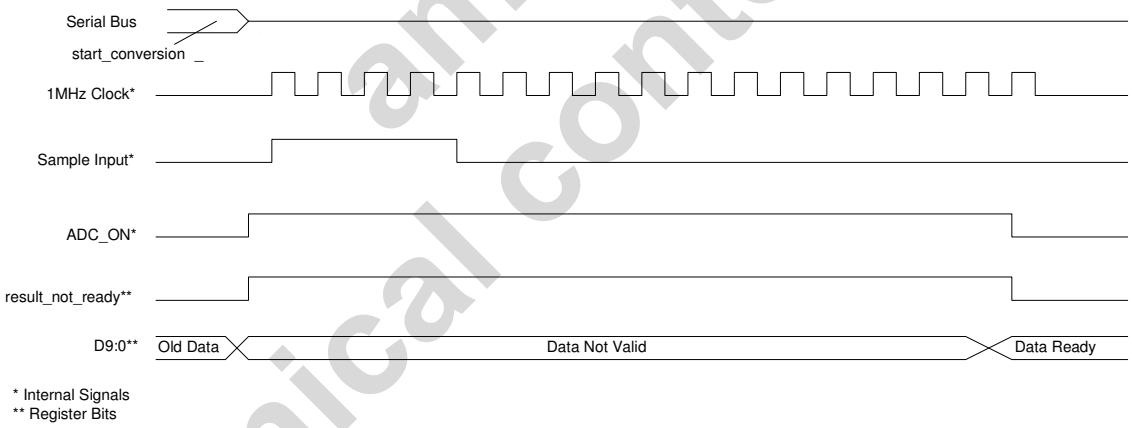
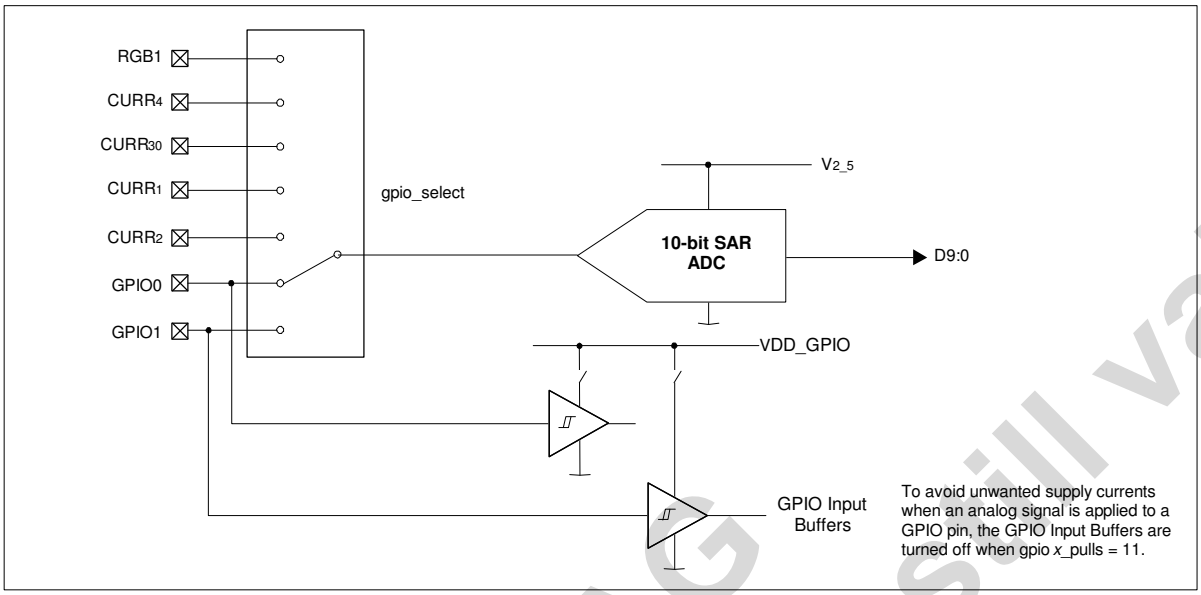


Figure 32 – ADC Pin Connections (TBD: TODO: Add new channels)



7.8 Power-On Reset

The internal reset is controlled by two sources:

- VBAT3 Supply
- VDD_GPIO Voltage

If one of the voltages is lower than its limit, the internal reset is forced.

The reset levels control the state of all registers. As long as VBAT and VDD_GPIO are below their reset thresholds, the register contents are set to default. Access by serial interface is possible once the reset thresholds are exceeded.

Table 23 – Reset Levels

Symbol	Parameter	Min	Typ	Max	Unit	Note
VPOR_VBAT	Overall Power-On Reset		2.0		V	Monitor voltage on V2_5; power-on reset for all internal functions; startup is guaranteed with VBAT>=3.0V
VGPIO_Vdd_TH_RISING	Reset Level for VDD_GPIO Rising		1.3	1.5	V	Monitor voltage on pin VDD_GPIO; rising level.
VGPIO_vdd_TH_FALLING	Reset Level for VDD_GPIO Falling		1.0		V	Monitor voltage on pin VDD_GPIO; falling level.

7.9 Temperature Supervision

An integrated temperature sensor provides over-temperature protection for the AS3688. This sensor generates a flag if the device temperature reaches the overtemperature threshold of 140º. The threshold has a hysteresis to prevent oscillation effects.

If the device temperature exceeds the 140º threshold all current sources, the charge pump, the ldo and the dcdc converter is disabled and the ov_temp flag is set. After decreasing the temperature by 5º (typically) operation is resumed.

The ov_temp flag can only be reset by first writing a 1 and then a 0 to the (bit rst_ov_temp).

Bit ov_temp_on = 1 activates temperature supervision.

Table 24 – Overtemperature Detection

Symbol	Parameter	Min	Typ	Max	Unit	Note
T140	ov_temp Rising Threshold		140		º C	
Thyst	ov_temp Hystersis		5		º C	

7.9.1 Temperature Supervision Registers

Addr: 29h		Overtemp Control		
		This register reads and resets the overtemperature flag.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	ov_temp_on	1	W	Activates/deactivates device temperature supervision. Default: Off – all other bits are only valid if this bit is set to 1. 0 = Temperature supervision is disabled. No reset will be generated if the device temperature exceeds 140ºC. 1 = Temperature supervision is enabled.
1	ov_temp	N/A	R	1 = Indicates that the overtemperature threshold has been reached; this flag is not cleared by an overtemperature reset. It has to be cleared using bit rst_ov_temp .
2	rst_ov_temp	0	R/W	The ov_temp flag is cleared by first setting this bit to 1, and then setting this bit to 0.
7:3				N/A

7.10 Serial Interface

The AS3688 is controlled using serial interface pins CLK and DATA.

7.10.1 Serial Interface Features

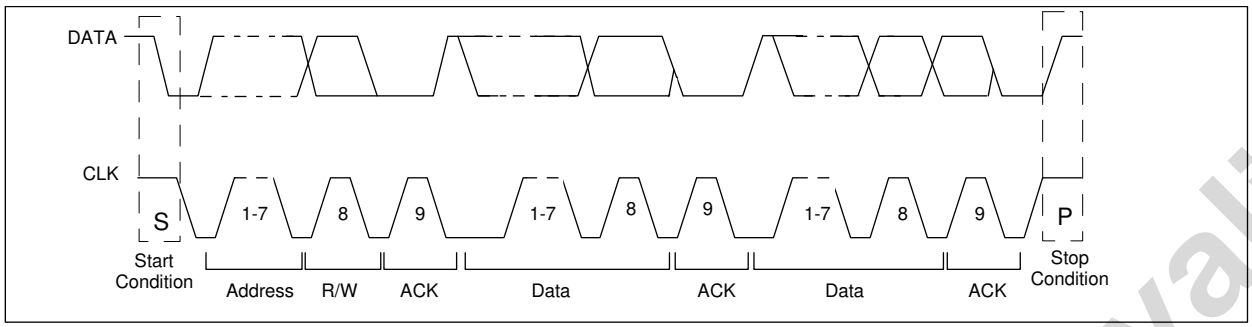
- Fast Mode Capability (Maximum Clock Frequency is 400 kHz)
- 7-bit Addressing Mode
- Write Formats
  - Single-Byte Write
  - Page-Write
- Read Formats
  - Current-Address Read
  - Random-Read
  - Sequential-Read
- DATA Input Delay and CLK Spike Filtering by Integrated RC Components

7.10.2 Device Address Selection

The serial interface address of the AS3688 has the following addresses (factory programmable to 80h,81h or 82h, 83h)

- 80h – Write Commands
- 81h – Read Commands

Figure 33 – Complete Serial Data Transfer



7.10.2.1 Serial Data Transfer Formats

Definitions used in the serial data transfer format diagrams are listed in the following table:

Table 25 – Serial Data Transfer Byte Definitions

Symbol	Definition	R/W (AS3688 Slave)	Notes
S	Start Condition after Stop	R	1 bit
Sr	Repeated Start	R	1 bit
DW	Device Address for Write	R	10000010b (80h).
DR	Device Address for Read	R	10000011b (81h)
WA	Word Address	R	8 bits
A	Acknowledge	W	1 bit
N	Not Acknowledge	R	1 bit
reg_data	Register Data/Write	R	8 bits
data (n)	Register Data/read	R	1 bit
P	Stop Condition	R	8 bits
WA++	Increment Word Address Internally	R	During Acknowledge

Figure 34 – Serial Interface Byte Write

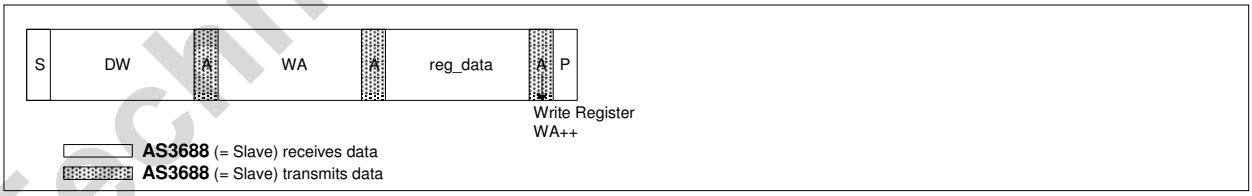
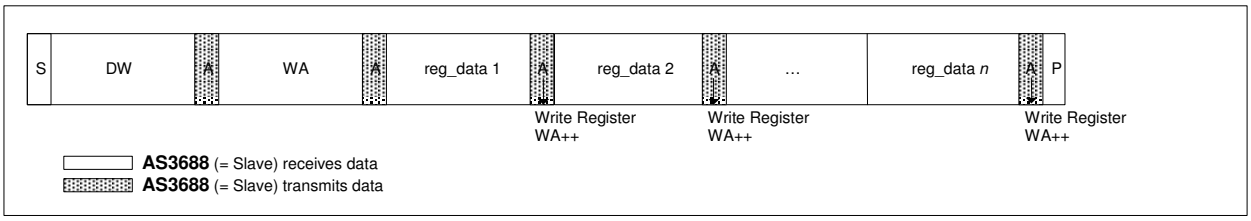


Figure 35 – Serial Interface Page Write



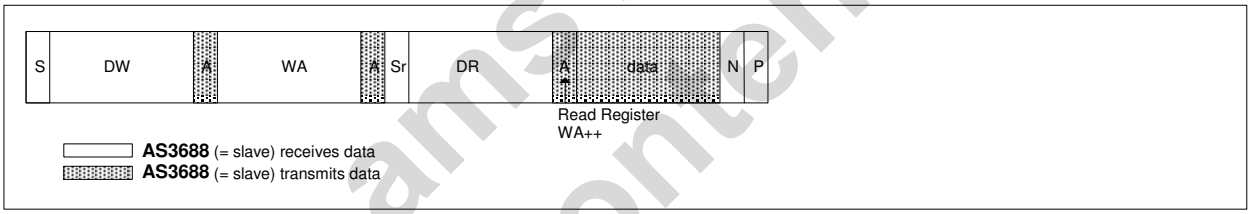
Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

The following diagrams show the serial read formats supported by the AS3688.

Figure 36 – Serial Interface Random Read

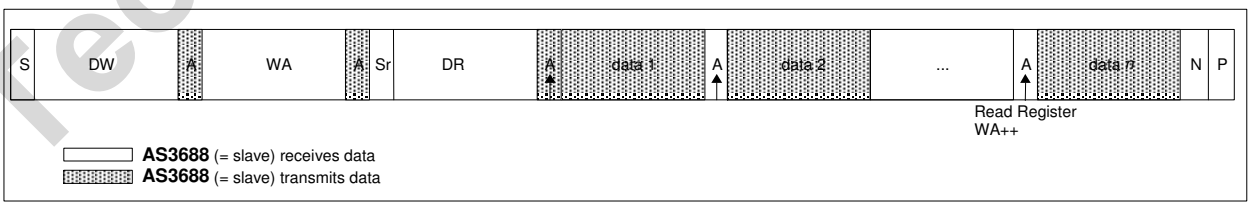


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st CLK pulse after the ACKNOWLEDGE bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a NOT ACKNOWLEDGE, and issues a STOP condition on the bus.

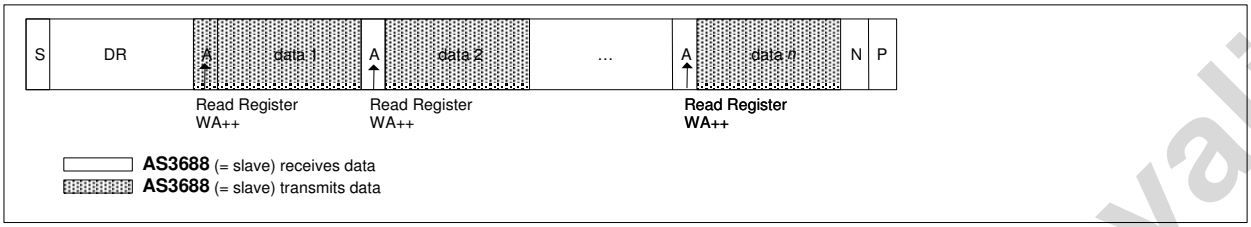
Figure 37 – Serial Interface Sequential Read



Sequential Read is the extended form of Random Read, as multiple register-data bytes are subsequently transferred.

In contrast to the Random Read, in a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a NOT ACKNOWLEDGE following the last data byte and subsequently generate the STOP condition.

Figure 38 – Serial Interface Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address.

Analogous to Random Read, a single byte transfer is terminated with a NOT ACKNOWLEDGE after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes must be responded to with an ACKNOWLEDGE from the master.

For termination of the transmission the master sends a NOT ACKNOWLEDGE following the last data byte and a subsequent STOP condition.

7.11 Operating Modes

If the voltage on VDD_GPIO is less than 0.3V, the AS3688 is in shutdown mode and its current consumption is minimized (I(BAT) = $I_{SHUTDOWN}$) and all internal registers are reset to their default values and the serial interface is disabled.

If the voltage on VDD_GPIO rises above 1.5V, the AS3688 serial interface is enabled and the AS3688 and the standby mode is selected.

If the LDO ANA1 is enabled (ldo_ana1_on=1) and ldo_ana1_lpo is set, the AS3688 enters low power mode (I(BAT) = $I_{LOWPOWER}$).

The AS3688 is switched automatically from standby mode (I(BAT) = $I_{STANDBY}$) or low power mode into normal mode (I(BAT) = I_{ACTIVE}) and back, if one of the following blocks are activated:

- LDO ANA1 in normal mode (ldo_ana1_lpo=0)
- LDO ANA2
- Charge pump
- External charge pump
- Step up regulator
- Any current sink
- ADC conversion started
- PWM active
- Pattern mode active.

If any of these blocks are already switched on (active mode) the internal oscillator is running and a write instruction to the registers is directly evaluated within 1 internal CLK Cycle (Typ. 1usec)

If all these blocks are disabled (standby mode or lowpower mode), a write instruction to enable these blocks is delayed by 64 CLK cycles (oscillator will startup, within max 200usec).

8 Registermap

Table 26 – Registermap

Register Name	Address	Default	Content b7	b6	b5	b4	b3	b2	b1	b0
Reg. control	00h	00	ldo_aa1_lpo			cp_ext_on	step_up_on	cp_on	ldo_aa2_on	ldo_ana1_on
curr12 control	01h	00h					curr2_mode		curr1_mode	
curr rgb control	02h	00h			rgb3_mode		rgb2_mode		rgb1_mode	
curr3 control1	03h	00h	curr33_mode		curr32_mode		curr31_mode		curr30_mode	
curr4 control	04h	00h			curr43_mode		curr42_mode		curr41_mode	
GPIO output	05h	00h	gpi_curr33_en	gpi_curr32_en	gpi_curr31_en	gpi_curr30_en	gpi_en	gpio2_out	gpio1_out	gpio0_out
GPIO signal	06h	00h	gpi_curr33_in	gpi_curr32_in	gpi_curr31_in	gpi_curr30_in	gpi_in	gpio2_in	gpio1_in	gpio0_in
Ldo ana1 voltage	07h	Fuse	ldo_ana1_voltage							
Ldo ana2 voltage	08h	Fuse			ldo_aa2_pulld	ldo_ana2_voltage				
Curr1 current	09h	00h	curr1_current							
Curr2 current	0Ah	00h	curr2_current							
Rgb1 current	0Bh	00h	rgb1_current							
Rgb2 current	0Ch	00h	rgb2_current							
Rgb3 current	0Dh	00h	rgb3_current							
Curr3x strobe	0Eh	00h	curr3x_strobe							
Curr3x preview	0Fh	00h	curr3x_preview							
Curr3x other	10h	00h	curr3x_other							
Curr3 strobe control	11h	00h	strobe_timing				strobe_mode		strobe_ctrl	
Curr3 control2	12h	00h		txmask_invert	curr3x_strobe_high	curr3x_ext_ovtemp	txmask_on	preview_ctrl		preview_off_after strobe
Curr41 current	13h	00h	curr41_current							
Curr42 current	14h	00h	curr42_current							
Curr43 current	15h	00h	curr43_current							
Pwm control	16h	01h		pwm_gpio2	pwm_dim_speed			pwm_dim_mode		pwm_mode
pwm code	17h	00h	pwm_code							
Pattern control	18h	00h	curr33_pattern	curr32_pattern	curr31_pattern	curr30_pattern	softdim_pattern	pattern_delay		pattern_color
Pattern data0	19h	00h	pattern_data[7:0]							
Pattern data1	1Ah	00h	pattern_data[15:8]							
Pattern data2	1Bh	00h	pattern_data[23:16]							
Pattern data3	1Ch	00h	pattern_data[31:24]							

Register Name	Address	Default	Content b7	b6	b5	b4	b3	b2	b1	b0
Ext. Charge pump mode	1Dh	00h				cp_ext_lowcurr	cp_ext_clk		cp_ext_mode	
GPIO01_control	1Eh	44h	gpio1_pulls		gpio1_mode		gpio0_pulls		gpio0_mode	
GPIO2_control	1Fh	0Ch					gpio2_pulls		gpio2_mode	
GPIO driving cap	20h	00h					gpio3_low_curr	gpio2_low_curr	gpio1_low_curr	gpio0_low_curr
DCDC control1	21h	00h	step_up_vtuning					step_up_fb		step_up_frequ
DCDC control2	22h	04h	step_up_fb_auto		curr2_prot_on	curr1_prot_on	step_up_lowcur	step_up_prot	skip_fast	step_up_res
CP control	23h	00h		cp_auto_on		cp_mode_switching		cp_mode		cp_clk
CP mode Switch1	24h	00h		rgb3_on_cp	rgb2_on_cp	rgb1_on_cp	curr33_on_cp	curr32_on_cp	curr31_on_cp	curr30_on_cp
CP mode Switch2	25h	00h				curr43_on_cp	curr42_on_cp	curr41_on_cp	curr2_on_cp	curr1_on_cp
ADC_control	26h	00h	start_conversion		adc_select					
ADC_MSB result	27h	NA	result_not_ready	D9	D8	D7	D6	D5	D4	D3
ADC_LSB result	28h	NA						D2	D1	D0
Overtemp control	29h	01h						rst_ov_temp	ov_temp	ov_temp_on
Curr low voltage status1	2Ah	NA		rgb3_low_v	rgb2_low_v	rgb1_low_v	curr33_low_v	curr32_low_v	curr31_low_v	curr30_low_v
Curr low voltage status2	2Bh	NA			ovtemp_ext	curr43_low_v	curr42_low_v	curr41_low_v	curr2_low_v	curr1_low_v
Gpio current	2Ch	00h	0	pattern_slow	0	0	gpio2_current			ext_ov_temp_inv
Adder Current 1	30h	00h	adder_current1 (can be enabled for RGB1, CURR41, CURR1)							
Adder Current 2	31h	00h	adder_current2 (can be enabled for RGB2, CURR42, CURR2)							
Adder Current 3	32h	00h	adder_current3 (can be enabled for RGB3, CURR43)							
Adder Enable 1	33h	00h			curr43_adder	curr42_adder	curr41_adder	rgb3_adder	rgb2_adder	rgb1_adder
Adder Enable 2	34h	00h							curr2_adder	curr1_adder
Subtract Enable	35h	00h						sub_en3	sub_en2	sub_en1
ASIC ID1	3Eh	C9h	1	1	0	0	1	0	0	1
ASIC ID2	3Fh	5xh	0	1	0	1	revision			

Note: If writing to register, write 0 to unused bits
Note: Write to read only bits will be ignored
Note: yellow color = read only

9 External Components

Table 27 – External Components List

Part Number	Value			Tol (min)	Rating (max)	Notes	Package (min)
	min	typ	max				
C1		100nF		+/-20%	6.3V	Ceramic, X5R (CREF)	0201
C2	1µF		4.7µF	+/-20%	6.3V	Ceramic, X5R (SENSES_P)	0603
C3		2.2µF		+/-20%	6.3V	Ceramic, X5R (VANA1) (e.g. Taiyo Yuden JDK105BJ225MV-F)	0402
C4	1µF		4.7µF	+/-20%	6.3V	Ceramic, X5R (V2_5) (e.g. Taiyo Yuden JMK105BJ105KV-F)	0402
C5		2.2µF		+/-20%	6.3V	Ceramic, X5R (VBAT1, VBAT2) (e.g. Taiyo Yuden JMK107BJ225MA-T)	0603
C6		2.2µF		+/-20%	6.3V	Ceramic, X5R (Charge Pump) (e.g. Taiyo Yuden JMK107BJ225MA-T)	0603
C7		2.2µF		+/-20%	6.3V	Ceramic, X5R (Charge Pump) (e.g. Taiyo Yuden JMK107BJ225MA-T)	0603
C8		2.2µF/ 4.7µF		+/-20%	6.3V	Ceramic, X5R (Charge Pump Output) (e.g. Taiyo Yuden JMK107BJ475MA-T) capacitor must have at least 1.5µF under all conditions	0603
C9		2.2µF		+/-20%	25V	Ceramic, X5R, X7R (Step Up DCDC converter output) (e.g. Taiyo Yuden TMK316BJ475KF)	1206
C10		1.5nF		+/-20%	25V	Ceramic, X5R (Step Up DCDC Feedback)	0402
C11		15nF		+/-20%	6.3V	Ceramic, X5R (Step Up DCDC Feedback) – not required for overvoltage detection	0402
C12		2.2µF		+/-20%	6.3V	Ceramic, X5R (RGB3/VANA2) (e.g. Taiyo Yuden JDK105BJ225MV-F) (only if VANA2 LDO is used)	0402
R1		220kΩ		+/-1%		Bias Resistor	0201
R2		100mΩ		+/-5%		Shunt Resistor	0805
R3		1MΩ		+/-1%		Step Up DC/DC Converter Voltage Feedback	0201
R4		100kΩ		+/-1%		Step Up DC/DC Converter Voltage Feedback – not required for overvoltage protection	0201
R5		1-10kΩ		+/-20%		Serial DATA line Pullup resistor	0201
R6						Light Sensor – optional	
L1		10µH		+/-20%		Recommended Type: Coiltronics SD- 12-100 or Panasonic ELLSFG100MA	

Part Number	Value			Tol (min)	Rating (max)	Notes	Package (min)
	min	typ	max				
D1	CMDSH2-3, BAT760 or similar					Shottky Diode; Central Semiconductor (CMDSH2-3) Philips, STM (BAT760)	SOD232
D2:D15	LED					As required by application	
Q1	Si1304, FDG313N or similar					NMOS switching transistor; Vishay (Si1304), Fairchild (FDG313N)	SOT-232

10 Pinout and Packaging

10.1 Pin Description

Table 28 – Pinlist QFN32

Pin	Name	Type	Description
1	GPI	DIO3	General purpose input
2	C2_N	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 2.2µF (±20%) to this pin.
3	VBAT2	S	Charge Pump supply pad. **Note:**Always connect this pin to VBAT.
4	C2_P	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 2.2µF (±20%) to this pin.
5	CP_OUT	AIO	Output voltage of the Charge Pump; connect a ceramic capacitor of 2.2µF (±20%) .
6	C1_P	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 2.2µF (±20%) to this pin.
7	VBAT1	AIO	Supply pad for Charge Pump. **Note:**Always connect this pin to VBAT.
8	C1_N	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 2.2µF (±20%) to this pin.
9	CURR33	AI	Analog current sink input (intended for LED flash).
10	CURR32	AI	Analog current sink input (intended for LED flash).
11	CURR31	AI	Analog current sink input (intended for LED flash).
12	CURR30	AI	Analog current sink input (intended for LED flash).
13	GPIO2	DIO3	General purpose input/output.
14	VDD_GPIO	S	Supply pad for GPIOs and serial interface.
15	GPIO1	DIO3	General purpose input/output, ADC input.
16	GPIO0	DIO3	General purpose input/output, ADC input.
17	CLK	DI3	Clock input for serial interface.
18	DATA	DIO3	Serial interface data input/output.
19	CURR1	AI_HV	Analog current sink input (intended for LED).
20	CURR2	AI_HV	Analog current sink input (intended for LED).
21	VANA1	AO	Output voltage of the Analog LDO VANA1. Connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%).
22	VBAT3	S	Supply pad; always connect to VBAT.
23	RGB3 (VANA2)	AI (AO)	RGB Current sink input Alternative function: Output voltage of the Analog LDO VANA2. Connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%) if this ldo is used.
24	SENSE_N (CURR43)	AIO	Negative sense input of shunt resistor for Step Up DC/DC Converter. Alternative function: General purposed current sink
25	SENSE_P (CURR42)	AIO	Positive sense input of shunt resistor for Step Up DC/DC Converter. Alternative function: General purposed current sink
26	DCDC_GATE	AO	DCDC gate driver.
27	RGB1	AI	RGB Current sink input
28	RGB2	AI	RGB Current sink input

Table 28 – Pinlist QFN32

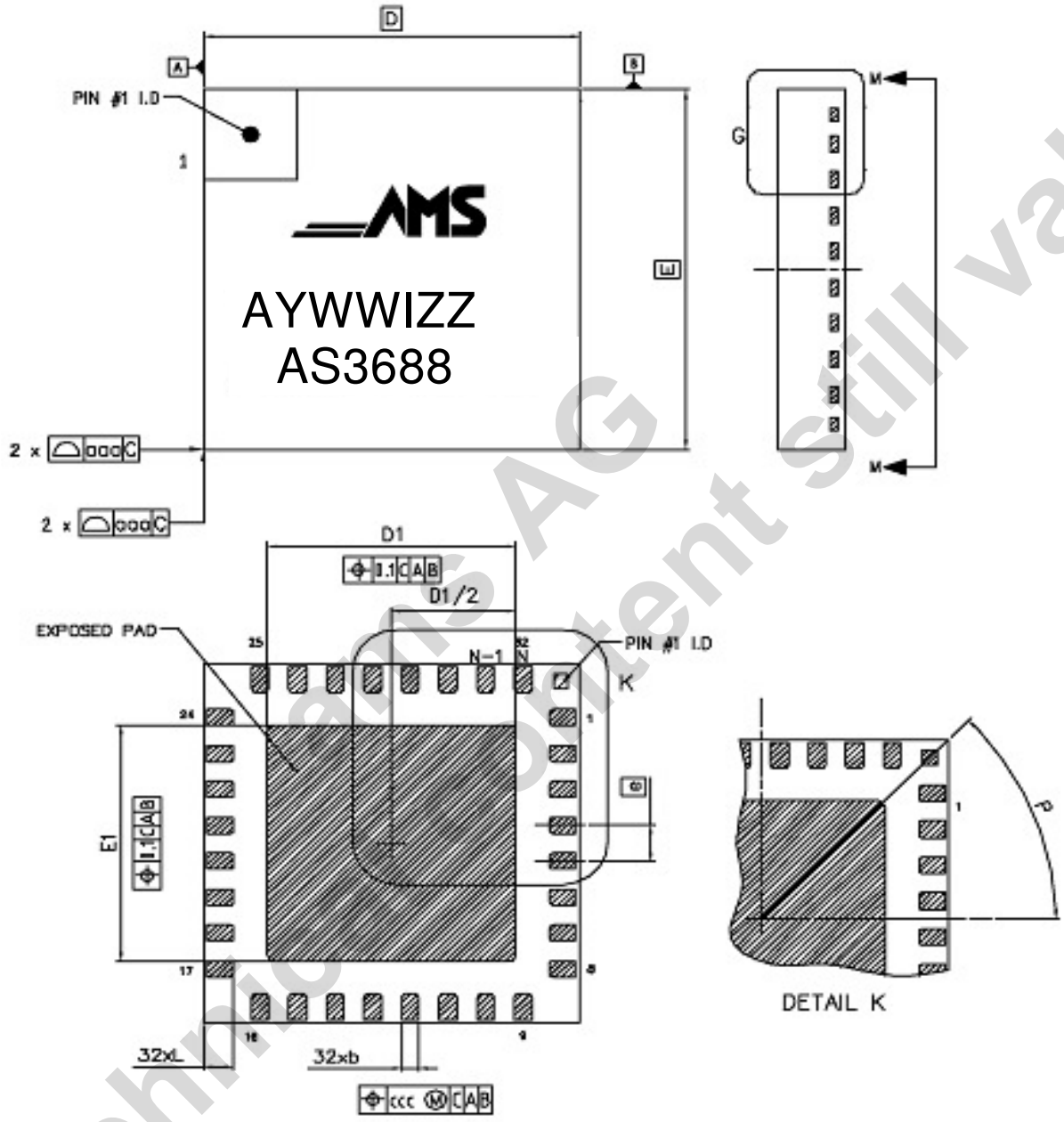
Pin	Name	Type	Description
29	DCDC_FB (CURR41)	AI	DCDC feedback. Connect to resistor string. Alternative function: General purposed current sink
30	V2_5	AO3	Output voltage of the Low-Power LDO; always connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%). **Caution:** Do not load this pin during device startup.
31	CREF	AIO	Bypass capacitor for the internal voltage reference; always connect a capacitor of 100nF. **Caution:** Do not load this pin.
32	RBIAS	AIO	External resistor; always connect a resistor of 220kΩ (±1%) to ground. **Caution:** Do not load this pin.
33	VSS	VSS	Ground pad (QFN32: exposed paddle).

Table 29 – Pin Type Definitions

Type	Description
DI	Digital Input
DI3	3.3V Digital Input
DO	Digital Output
DIO	Digital Input/Output
DIO3	3.3V Digital Input/Output
OD	Open Drain (the device can only pulldown this type of pin)
AIO	Analog Pad
AI	Analog Input
AI_HV	High-Voltage (15V) Pin
AO	Analog Output (5V)
AO3	Analog Output (3.3V)
S	Supply Pad
GND	Ground Pad

10.2 Package Drawings and Markings

Figure 39 – QFN 32 – 5x5mm with Exposed Paddle

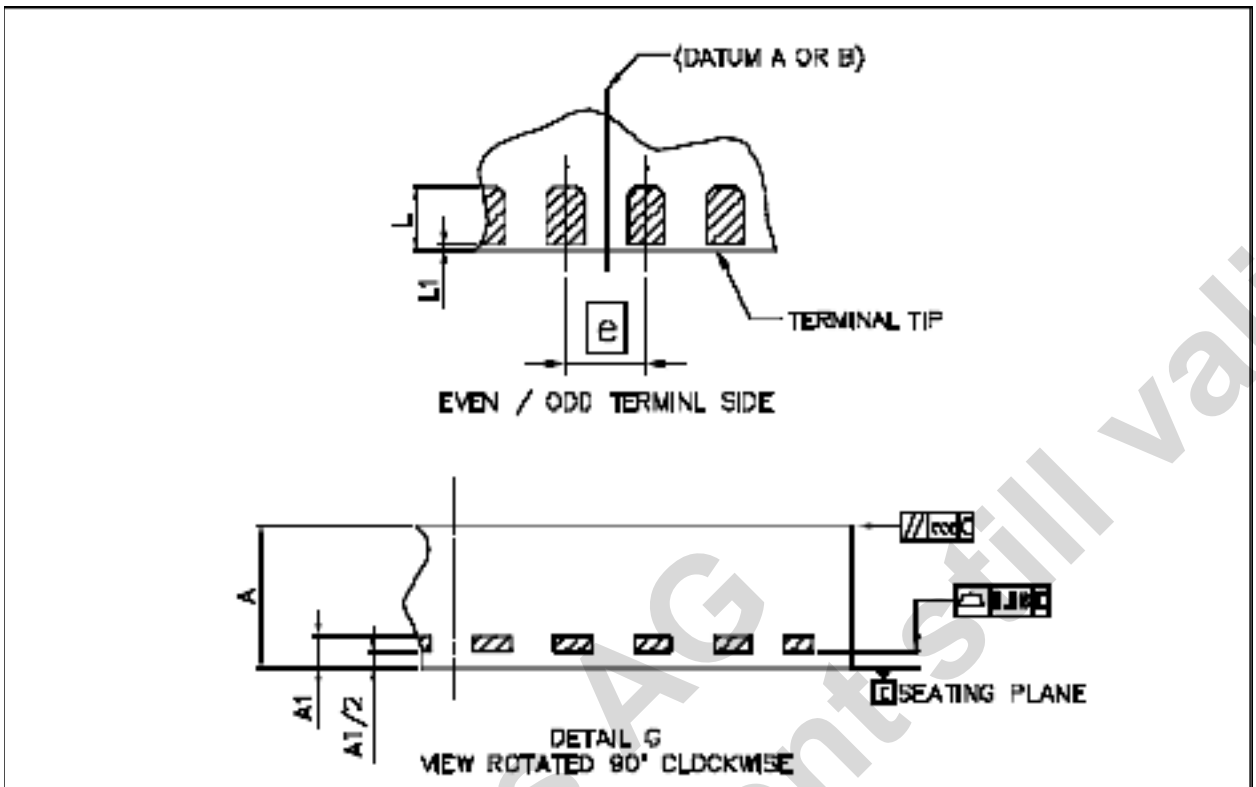


JEDEC Package Outline Standard: MO-220 VHHD-5 – Lead Finish: 100% Sn "Matte Tin".

Marking: AYWWIZZ

A: Pb-Free Identifier
Y: Last Digit of Manufacturing Year
WW: Manufacturing Week
I: Plant Identifier
ZZ: Traceability Code

Figure 40 – QFN 32 – Detail Diagram



DIM	MIN	NOM	MAX
A	0.80		1.00
A1		0.203 REF	
b	0.18	0.23	0.30
D		5.00 BSC	
E		5.00 BSC	
D1	3.50	3.60	3.70
E1	3.50	3.60	3.70
e		0.50 BSC	
L	0.30	0.40	0.50
L1			0.10
P		45° BSC	
aaa		0.15	
ccc		0.10	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

UNIT	DIMENSION AND TOLERANCE	REFERENCE DOCUMENT
Millimeter(mm)	ASME Y14.5M	JEDEC MO-220

11 Ordering Information

Device ID	Part Number	Package Type	Delivery Form*	Description
AS3688-PDR-Z	AS3688-EAA-Z	QFN 32	Tape and Reel	5 x 5mm, Pitch = 0.5mm
	AS3688-EBA-Z	QFN 32	Tube	5 x 5mm, Pitch = 0.5mm
AS3688B-PDR-Z	AS3688B-EAA-Z	QFN 32	Tape and Reel	5 x 5mm, Pitch = 0.5mm; version with CURR42 and CURR43 current source but without dcdc converter
	AS3688B-EBA-Z	QFN 32	Tube	

Where:

P = **Package Type**:

E = QFN 5 x 5 x 1mm

D = **Delivery Form**:

A = Tape and Reel

B = Tube

R = **Revision**

Z = **Pb-Free IC Package**

* Dry-pack sensitivity level = 3 in accordance with *IPC/JEDEC J-STD-033A.*

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