Product Document

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TMD2621

Proximity Sensor Module for Behind OLED Applications

General Description

The TMD2621 features an advanced proximity measurement. The device integrates an IR VCSEL and an advanced VCSEL driver within an optimized 4.65mm x 1.86mm x 1.3mm OLGA package.

The proximity function synchronizes IR emission and detection to sense nearby objects. The architecture of the engine features self-maximizing dynamic range, ambient light subtraction, advanced crosstalk cancellation, and interrupt-driven I^2C communication. Sensitivity, power consumption, and noise can be optimized with adjustable IR VCSEL timing and power. The proximity engine recognizes detect/release events and produces a configurable interrupt whenever the proximity result crosses upper or lower threshold settings.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TMD2621 are listed below:

Figure 1:
Added Value of Using TMD2621

Benefits	Features
• Proximity detection behind OLED displays	• Integrated factory calibrated 940nm IR VCSEL • Display synchronization with highly programmable Proximity Start Delay (PSD) • Crosstalk and ambient light cancellation • Optimized sensitivity and noise level • Wide configuration range
• Low power consumption	• 1.8V power supply with 1.8V I^2C bus • Configurable sleep mode • Interrupt driven device
• Integrated status checking for all functions	• Proximity saturation flag • VSYNC status check

Applications

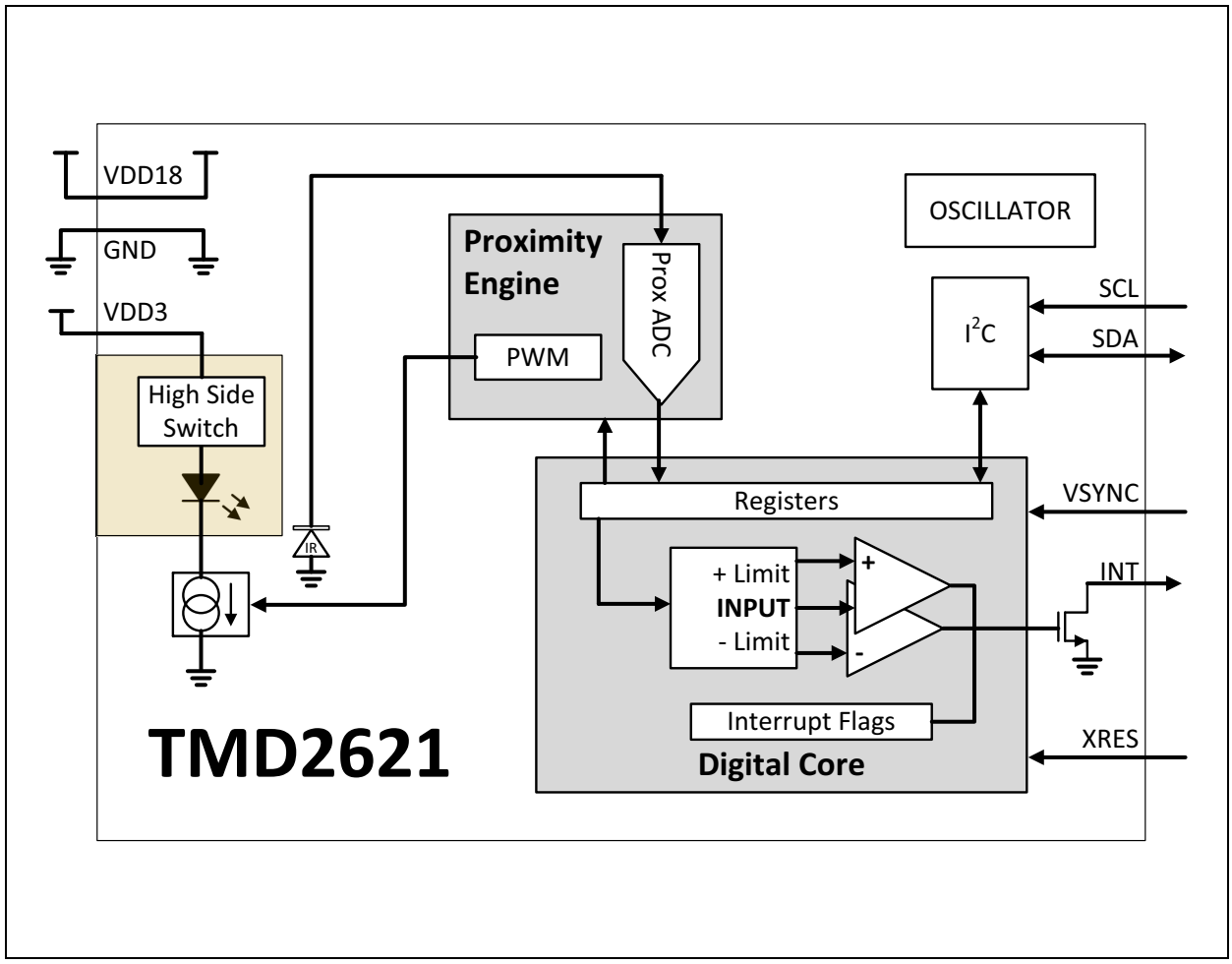
The TMD2621 applications include:

- Proximity detection for mobile phones

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TMD2621



Pin Assignments

Figure 3:
Pin Diagram

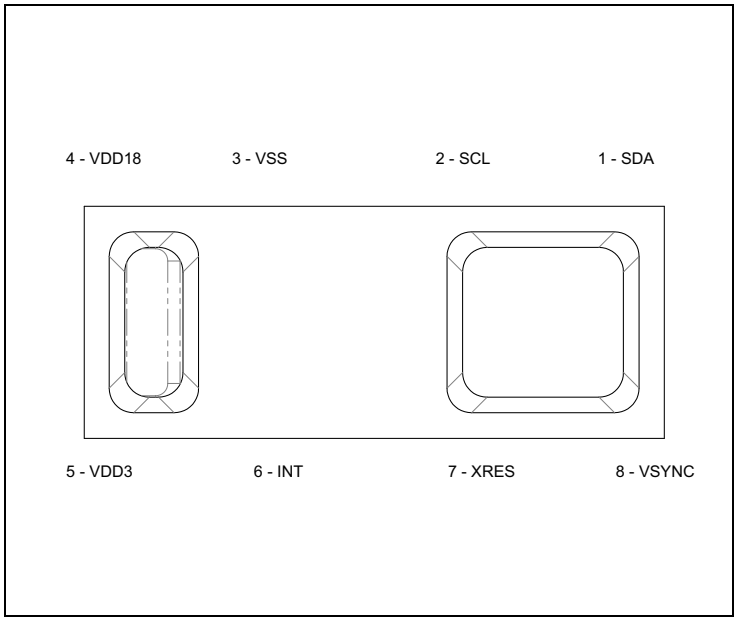


Figure 4:
Pin Description of TMD2621

PIN Number	Pin Name	Description	If Not Use
1	SDA	I^2C serial data I/O terminal.	Mandatory
2	SCL	I^2C serial clock input terminal.	Mandatory
3	VSS	Ground. All voltages are referenced to VSS.	Mandatory
4	VDD18	Supply voltage for sensor (1.8V).	Mandatory
5	VDD3	Supply voltage for IR emitter (3.0/3.3V).	Connect to VDD18
6	INT	Interrupt. Open drain output (active low).	Connect to GND
7	XRES	Hardware reset input. Need to enable in the register.	Connect to GND
8	VSYNC	VSYNC input.	Connect to GND

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD18	Supply voltage to GND	-0.3	1.98	V	
VDD3	IR emitter voltage to GND	-0.3	3.6	V	
V_{IO}	Digital I/O terminal voltage	-0.3	3.6	V	INT, XRES, VSYNC, SDA, SCL
I_{IO}	Digital output terminal current	-1	20	mA	
Electrostatic Discharge					
I_{SCR}	Input current (latch-up immunity)	± 100		mA	JEDEC JESD78E Class II
ESD_{HBM}	HBM electrostatic discharge	± 2000		V	ANSI/ESDA/JEDEC JS-001-2017
ESD_{CDM}	CDM electrostatic discharge	± 500		V	ANSI/ESDA/JEDEC JS-002-2018
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage temperature range	-40	85	°C	
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.”
RH_{NC}	Relative humidity (non-condensing)		85	%	
MSL	Moisture sensitivity level	3			Represents a max. floor life time of 168h

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD18	Supply voltage to sensor	1.7	1.8	1.98	V
VDD3	Supply voltage to IR emitter	2.9	3.3	3.6	V
T_A	Operating ambient temperature (1)	-30		85	°C

Note(s):

1. While the device is operational across the temperature range, performance will vary with temperature. Operational characteristics are at 25°C, unless otherwise noted.

Figure 7:
Operating Characteristics, VDD18 = 1.8V, VDD3=3.0V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Oscillator frequency		7.9	8.1	8.3	MHz
I_{DD}	Supply current (1)	Active Proximity State (PON=PEN=1) (2)		584	684	µA
		Idle State (PON=1, PEN=0) (3)		76	100	
		Sleep State (PON = 0) (4)		0.7	5	
V_{OL}	INT, SDA output low voltage	6mA sink current			0.6	V
I_{LEAK}	Leakage current, SDA, SCL, INT		-5		5	µA
V_{IH}	SCL, SDA, VSYNC, XRES input high voltage		1.26			V
V_{IL}	SCL, SDA, VSYNC, XRES input low voltage				0.54	V
T_{Active}	Time from power-on to ready to receive I^2C commands			1.6		ms

Note(s):

1. Values are shown at the VDD18 pin and do not include current through the IR VCSEL emitter.
2. Active state occurs when PON =1 and the device is actively integrating.
3. Idle state occurs when PON=1 and all functions are not enabled.
4. Sleep state occurs when PON = 0 and I^2C bus is idle. If sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.

Optical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (statistical Quality Control) methods. Device parameters are guaranteed with V_{DD18}=1.8V, V_{DD3}=3.0V and T_A=25°C unless otherwise noted.

Figure 8:
Proximity Optical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Response: Absolute (1)	PTIME =528µs PGAIN =2x; PGAIN2 =2.5x PLDRIVE0 =10mA PPULSE =1pulse PPULSE_LEN =45µs PROX_DATA_AVG =8 BINSRCH_TARGET =15 APC = Disabled ORE = Disabled Electrical Calibration No glass above module Target Material: 18% reflective surface Target Size: 100mm x 100mm Target Distance: 30mm		854		counts
Part to Part Variation (2)	Same as Response: Absolute except the target is 2 inch diameter broadband diffusor with target distance of 85.75mm			±25	%
Response: No Target (3)	Same as Response: Absolute except no target		14		counts
Noise/Signal (4)	Same as Response: Absolute except the target is 2 inch diameter broadband diffusor with target distance of 85.75mm		0.115	2	%

Note(s):

1. Representative result by lab characterization with VDD3 = 3.3V.
2. Optically trimmed at factory final test.
3. Response with no target varies with power supply characteristics and system noise.
4. Production tested results is the standard deviation of 10 readings divided by the average response.

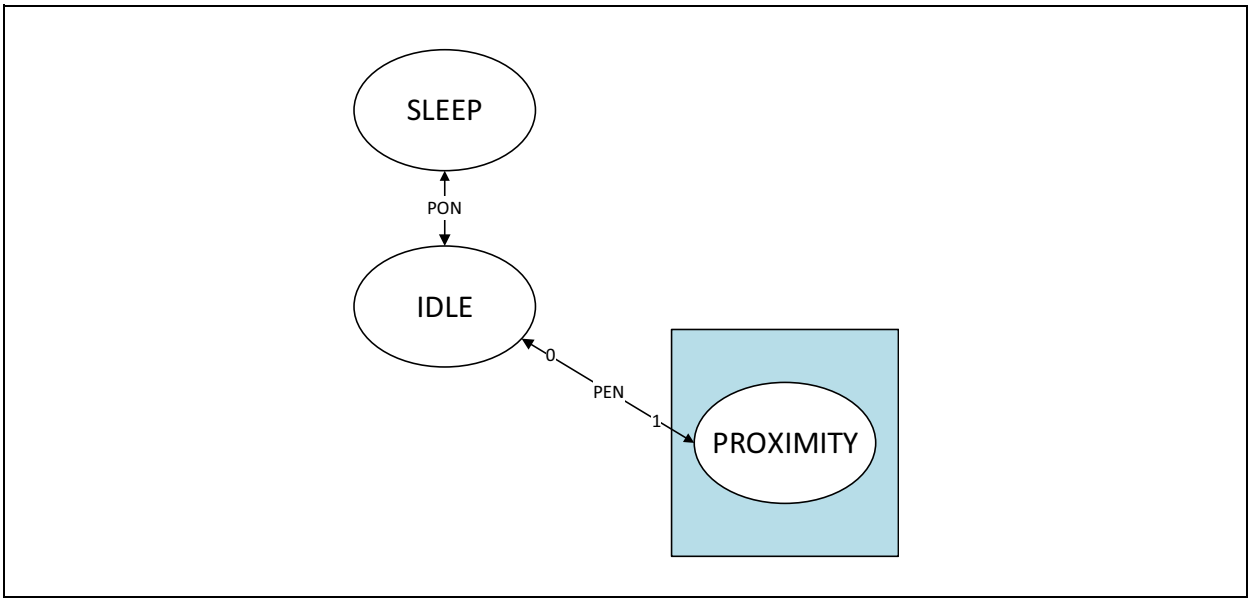
Detailed Description

Power Up

Upon power-up, device initialization occurs. During initialization, the device cannot accept I²C transactions and will deterministically send NAK for any I²C requests. All communication with the device must be delayed, and all outputs from the device (i.e. interrupts) must be ignored until initialization completes. After initialization, the device enters the SLEEP state in which the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If an I²C transaction occurs during the SLEEP state, the I²C core wakes up temporarily to service the communication. When the Power ON bit, PON, is enabled, the device enters the IDLE state in which the internal oscillator and attendant circuitry are active, but power consumption remains low. After PON is set, there is a 100µs wait time required before enabling PEN. This allows the device time to settle the internal node voltages and currents before starting the Proximity measurements. When proximity measurement is enabled (PEN=1), the device exits the IDLE state. When the function is disabled (PEN=0), the device returns to the IDLE state.

Figure 9 shows the simplified state diagram of TMD2621. When a proximity calibration is requested, it will take precedence over the proximity measurement function. If Sleep After Interrupt is enabled (SAI = 1 in register 0xAB), the state machine will enter SLEEP when an interrupt occurs. Entering SLEEP will not change any of the register settings (e.g. PON will still be high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated when the interrupt status register is cleared (the status bit is in register 0xA0-0xA1).

Figure 9:
Simplified State Diagram



Proximity

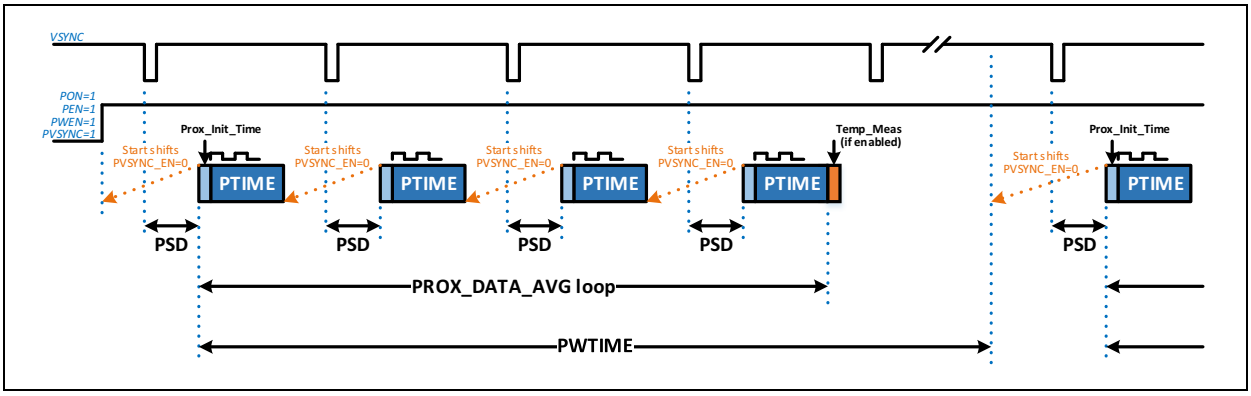
The proximity system consists of an IR VCSEL and its driver generating periodic IR pulses which are reflected and received by the proximity photodiode and modulator sub-system. The reflected energy is measured by integrating the photodiode current and translating it to an ADC input voltage. The presence of a reflective object at some distance can be extracted as a function of ADC output data which represents the reflected signal intensity.

Proximity results are affected by three fundamental factors: the integrated IR VCSEL emission, IR reception (signal + crosstalk), and environmental factors, including target distance and surface reflectivity. The IR reception signal path begins with IR detection from a photodiode and ends with the 14-bit proximity result in PDATA register. Signal from the photodiode is amplified, and offset adjusted to optimize performance. Offset correction or crosstalk compensation is accomplished by adjustment to the POFFSET register. The analog circuitry of the device applies the offset value as a subtraction to the signal accumulation, therefore a positive offset value has the effect of decreasing the PDATA value. The integrated offset calibration feature performs this crosstalk compensation.

The proximity IR VCSEL emission is designed to be able to synchronize to the display VSYNC signal with a delay time defined by PSD when PVSYNC_EN=1. PTIME defines the duration of one proximity sample. PTIME needs to be programmed to a value greater than the sample integration time, otherwise it will be ignored. Using PTIME, proximity sample timing can be programmed to skip VSYNC periods. The device hardware allows to collect and average multiple proximity samples for a single proximity measurement result by programming the PROX_DATA_AVG register. Device temperature is measured and updated in the TDATA register after every proximity measurement cycle when TEN=1 and ENAB_TEMP_SENSOR =1. PWTIME provides the ability to add wait time and defines the repetition period of one proximity measurement cycle. The subsequent proximity cycle will occur on the first VSYNC after the end of the PWTIME period, plus the delay defined by PSD.

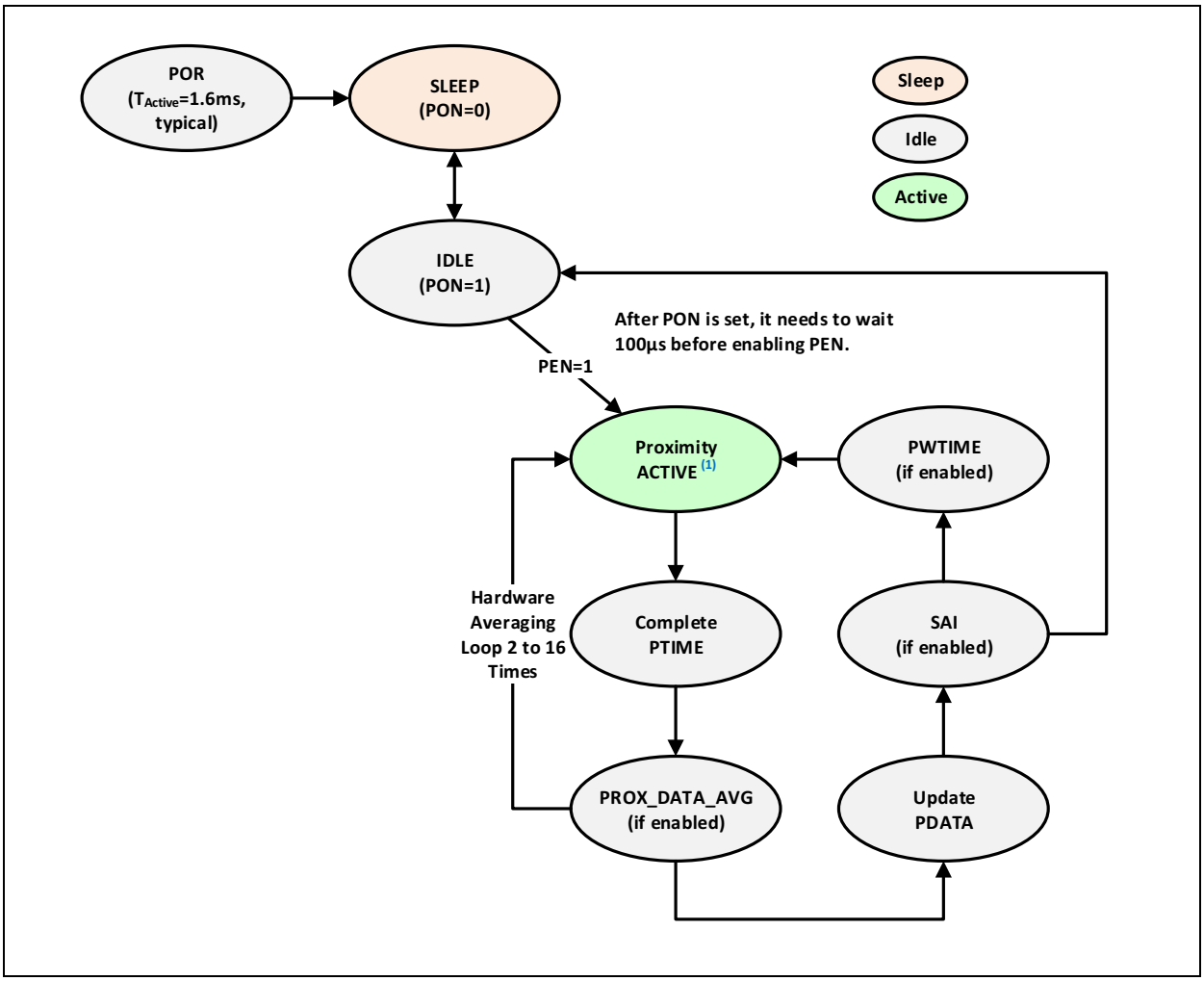
Figure 10 shows an example of proximity integration and data sampling for the TMD2621.

Figure 10:
Proximity Integration and Data Sampling in TMD2621



Operational State Diagram

Figure 11:
Operational State Diagram



Note(s):

1. Proximity active time = PPULSE x (2 x (PPULSE_LEN + 42.15µs)) + 78.75µs.
2. All numbers in the above equation are typical values.

I²C Protocol

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and fast clock frequency modes. Read and write transactions comply with the standard set by Philips (now NXP).

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address + 1.

I²C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESS$_{WRITE}$, REGISTER-ADDRESS, DATA BYTE(S), and STOP. Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/ NOT-ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

I²C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESS$_{WRITE}$, REGISTER-ADDRESS, START, CHIP-ADDRESS$_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Alternately, if the previous I²C transaction was a Read, the internal register address buffer is still valid, allowing the transaction to proceed without “re”-specifying the register address. In this case the transaction consists of a START, CHIP-ADDRESS$_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the

NXP I²C design specification at:

https://www.i2c-bus.org/references/

I²C Timing Characteristics

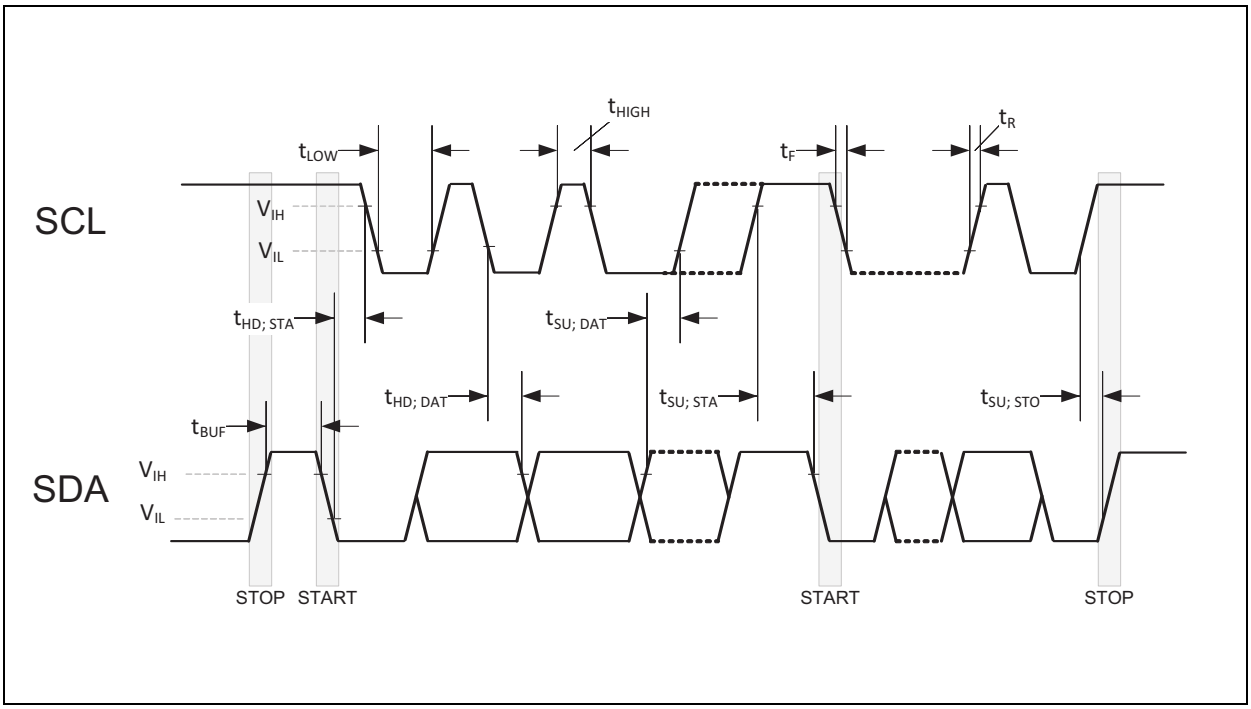
The timing parameters are specified by design and characterization and are not production tested unless otherwise noted. All parameters are measured with V_{DD} = 1.8V and T_A = 25°C unless otherwise noted.

Figure 12:
I²C Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	I²C clock frequency	0		400	kHz
t_{BUF}	Bus free time between start and stop condition	1.3			µs
$t_{HD;STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated	0.6			
$t_{SU;STA}$	Repeated start condition setup time	0.6			
$t_{SU;STO}$	Stop condition setup time	0.6			
t_{LOW}	SCL clock low period	1.3			
t_{HIGH}	SCL clock high period	0.6			
$t_{HD;DAT}$	Data hold time	0			ns
$t_{SU;DAT}$	Data setup time	100			
t_F	Clock/data fall time			300	
t_R	Clock/data rise time			300	

I²C Timing Diagram

Figure 13:
I²C Timing Diagram



Register Overview

The device is controlled and monitored by registers accessed through the I²C serial interface. These registers provide device control functions and are read to determine device status and acquire device data.

Register Map

The register set is summarized in Register Map. The values of all registers and fields that are listed as reserved or are not listed must not be changed at any time. The power-on reset values of each bit are indicated in these columns. Two-byte fields are always latched with the low byte followed by the high byte.

Figure 14:
Register Map

Address	Register Name	Type	Description	Reset
0x07	LOTL	R	Lot ID low byte	0x00
0x08	LOTH	R	Lot ID high byte	0x00
0x09	SNL	R	Serial number low byte	0x00
0x0A	SNH	R	Serial number high byte	0x00
0x1A	IPTAT	RW	IPTAT code	0x07
0x80	ENABLE	RW	Enables device states	0x00
0x82	PTIME	RW	Proximity time	0x1F
0x88	PILTL	RW	Proximity interrupt low threshold low byte	0x00
0x89	PILTH	RW	Proximity interrupt low threshold high byte	0x00
0x8A	PIHTL	RW	Proximity interrupt high threshold low byte	0x00
0x8B	PIHTH	RW	Proximity interrupt high threshold high byte	0x00
0x8C	PERS	RW	Proximity interrupt persistence filters	0x00
0x8D	CFG0	RW	Configuration zero	0x10
0x8E	PCFG0	RW	Proximity configuration zero	0x43
0x8F	PCFG1	RW	Proximity configuration one	0x00
0x90	PCFG2	RW	Proximity configuration two	0x20
0x91	REVID	R	Revision ID	0x11
0x92	ID	R	Device ID	0x82
0x93	REVID2	R	Auxiliary ID	0x05
0x94	CFG1	RW	Configuration one	0x00
0x9A	LDR0_CFG	RW	Proximity LDR0 drive strength configuration	0x52

Address	Register Name	Type	Description	Reset
0x9E	EYE_SAFETY_CFG	RW	Eye safety configuration	0x40
0x9F	EYE_SAFETY_STATUS	R	Eye safety status	0x00
0xA0	STATUS	R, SC	Device status	0x00
0xA1	STATUS_2	R, SC	Device status two	0xC0
0xA7	CFG2	RW	Configuration two	0x43
0xA8	RESET	RW	RESET	0x00
0xAB	CFG3	RW	Configuration three	0x41
0xAE	CFG6	RW	Configuration six	0x76
0xB1	VSYNC_CFG	RW	VSYNC configuration	0x00
0xB2	VSYNC_PRD_L	RW	VSYNC period low data	0x00
0xB3	VSYNC_PRD_H	RW	VSYNC period high data	0x00
0xC0	POFFSET	RW	POFFSET data	0x00
0xC1	POFFSET_SIGN	RW	POFFSET sign	0x00
0xD7	CALIB	RW	Proximity offset calibration	0x00
0xD8	CALIB_OFFSET	RW	Proximity offset extension	0x00
0xD9	CALIBCFG	RW	Proximity offset calibration control	0x50
0xDA	PCFG4	RW	Proximity configuration four	0x00
0xDC	CALIBSTAT	R	Proximity offset calibration status	0x00
0xDD	INTENAB	RW	Interrupt enables	0x00
0xDE	INTENAB_2	RW	Interrupt enables two	0x00
0xEA	PSD_L	RW	Proximity start delay low data	0x00
0xEB	PSD_H	RW	Proximity start delay high data	0x00
0xEC	PWTIME	RW	Proximity wait time	0x00
0xF4	PDATA_L	R	Proximity low data	0x00
0xF5	PDATA_H	R	Proximity high data	0x00
0xF6	TDATA_L	R	Temperature low data	0x00
0xF7	TDATA_H	R	Temperature high data	0x00

Note(s):

1. R = Read Only; WO = Write Only; RW = Read or Write; SC = Self Clearing after access.

Detailed Register Description

LOTL Register (Address 0x07)

Figure 15:
LOTL Register

Addr: 0x07		LOTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	LOTL	0x00	R	The low byte of the 16-bit lot ID.

LOTH Register (Address 0x08)

Figure 16:
LOTH Register

Addr: 0x08		LOTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	LOTH	0x00	R	The high byte of the 16-bit lot ID.

SNL Register (Address 0x09)

Figure 17:
SNL Register

Addr: 0x09		SNL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SNL	0x00	R	The low byte of the 16-bit serial number.

SNH Register (Address 0x0A)

Figure 18:
SNH Register

Addr: 0x0A		SNH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SNH	0x00	R	The high byte of the 16-bit serial number.

IPTAT Register (Address 0x1A)

Figure 19:
IPTAT Register

Addr: 0x1A		IPTAT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Reserved	000	RW	Reserved. Must be set to default value.
4:0	IPTAT	00111	RW	The IPTAT value needs to be changed from its default value to be “00011b” during device initialization.

Enable Register (Address 0x80)

Figure 20:
ENABLE Register

Addr: 0x80		ENABLE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PVSYNC_EN	0	RW	This bit enables proximity integration synced with VSYNC.
6	Reserved	0	RW	Reserved. Must be set to default value.
5	TEN	0	RW	This bit activates temperature measurement after every proximity measurement.
4	PWEN	0	RW	This bit activates the proximity wait feature which is set by the PWTIME register. Active high.
3	Reserved	0	RW	Reserved. Must be set to default value.
2	PEN	0	RW	This bit activates the proximity detection. Active high.
1	Reserved	0	RW	Reserved. Must be set to default value.
0	PON	0	RW	Power ON. This field activates the internal oscillator and ADC channels. Active high.

Preset each applicable registers and its bits as per required operation before activating PON. After PON is set, it is required to wait 100µs settling time and then enable PEN. In order to modify register configurations during operation, it is required to set PEN=PON=0 firstly to avoid any unexpected behavior or corrupted proximity results. Disabling PON resets the device state machine, but all the register values will retain. After the configuration change done, set the PON bit and wait 100µs settling time, and then enable PEN to re-activate the corresponding functionalities.

PTIME Register (Address 0x82)

Figure 21:
PTIME Register

Addr: 0x82		PTIME		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PTIME	0x1F	RW	This register defines the duration of 1 Prox Sample, which is (PTIME + 1)*88µs. PTIME needs to be programmed greater than proximity integration time, otherwise it's ignored.

PILTL Register (Address 0x88)

Figure 22:
PILTL Register

Addr: 0x88		PILTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PILTL	0x00	RW	This register contains the low byte of the 14-bit proximity LOW threshold when APC is enabled. If APC is disabled, this register contains the LOW threshold which is an 8-bit value which is compared against the upper 8 bits of the 10-bit proximity value.

PILTH Register (Address 0x89)

Figure 23:
PILTH Register

Addr: 0x89		PILTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	00	RW	Reserved. Must be set to default value.
5:0	PILTH	000000	RW	This register contains the upper 6 bits of the 14-bit proximity LOW threshold when APC is enabled. If APC is disabled, this register is ignored.

The contents of the PILTH and PILTL registers are combined and treated as a fourteen (14) bit threshold low value. If the value generated by the proximity ADC (PDATA) is below the PILTL/H threshold and the PPERS value is reached, then the low proximity threshold is breached. When setting the 14-bit proximity threshold, PILTL must be written first, immediately follow by PILTH. Internally, the lower 8 bits are buffered until

the upper 8 bits are written. As the upper 8 bits are written both the high and low bytes are simultaneously latched as a 14-bit value.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then the proximity data converts to a 10-bit value. PILTL contains an 8-bit threshold which is compared against the upper 8 bits of the 10-bit value. PILTH is ignored.

PIHTL Register (Address 0x8A)

Figure 24:
PIHTL Register

Addr: 0x8A		PIHTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PIHTL	0x00	RW	This register contains the low byte of the 14-bit proximity HIGH threshold when APC is enabled. If APC is disabled, this register contains the HIGH threshold which is an 8-bit value which is compared against the upper 8 bits of the 10-bit proximity value.

PIHTH Register (Address 0x8B)

Figure 25:
PIHTH Register

Addr: 0x8B		PIHTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	00	RW	Reserved. Must be set to default value.
5:0	PIHTH	000000	RW	This register contains the upper 6 bits of the 14-bit proximity HIGH threshold when APC is enabled. If APC is disabled, this register is ignored.

The contents of the PIHTH and PIHTL registers are combined and treated as a fourteen (14) bit threshold high value. If the value generated by the proximity ADC (PDATA) is above the PIHTL/H threshold and the PPERS value is reached, then the high proximity threshold is breached. When setting the 14-bit proximity threshold, PIHTL must be written first, immediately follow by PIHTH. Internally, the lower 8 bits are buffered until the upper 8 bits are written. As the upper 8 bits are written both the high and low bytes are simultaneously latched as a 14-bit value.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then the proximity data converts to a 10-bit value. PIHTL contains an 8-bit threshold which is compared against the upper 8 bits of the 10-bit value. PIHTH is ignored.

PERS Register (Address 0x8C)

Figure 26:
PERS Register

Addr: 0x8C		PERS			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:4	PPERS	0000	RW	This register sets the proximity persistence filter.	
				Value	**Interrupt**
				0	Every proximity cycle
				1	Any value outside proximity thresholds
				2	2 consecutive proximity values out of range
				3	3 consecutive proximity values out of range
				…	….
				15	15 consecutive proximity values out of range
3:0	Reserved	0000	RW	Reserved. Must be set to default value.	

The frequency of consecutive proximity channel results outside of threshold limits are counted; this count value is compared against the PPERS value. If the counter is equal to the PPERS value an interrupt is asserted. Any time a proximity channel result is inside the threshold values the counter is cleared.

CFG0 Register (Address 0x8D)

Figure 27:
CFG0 Register

Addr: 0x8D		CFG0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ENAB_16_ BIT_OP	0	RW	Enables output of PDATA to be a 16-bit value when APC is ON. See PDATA (0xF4 and 0xF5) for details.
6:4	Reserved	001	RW	Reserved. Must be set to default value.
3	PWLONG	0	RW	When PWLONG (PROX Wait Long) is asserted the wait period as set by PWTIME is increased by a factor of 12.
2:0	Reserved	000	RW	Reserved. Must be set to default value.

PCFG0 Register (Address 0x8E)

Figure 28:
PCFG0 Register

Addr: 0x8E		PCFG0			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	PGAIN	010	RW	This field sets proximity first stage gain control.	
				Value	**Stage 1 Gain**
				0 (000)	1x
				1 (001)	2x
				2 (010)	4x
				3 (011)	8x
				4 (100)	16x
4:2	Reserved	000	RW	Reserved. Must be set to default value.	
1:0	PGAIN2	11	RW	This field sets proximity second stage gain control.	
				Value	**Stage 2 Gain**
				0 (00)	2.5x
				1 (01)	5x
				2 (10)	Reserved, must not use.
				3 (11)	10x

PCFG1 Register (Address 0x8F)

Figure 29:
PCFG1 Register

Addr: 0x8F		PCFG1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	PPULSE_LENH	00	RW	These bits are the 2 most significant bits of the 10-bit Pulse Length control setting. The lower 8 bits are in the PCFG2 register. See the PCFG2 register for details.

Addr: 0x8F		PCFG1			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
5:0	PPULSE	000000	RW	Maximum number of pulses in a single proximity cycle.	
				Value	**Maximum Number of Pulses**
				0 (000000)	1
				1 (000001)	2
				2 (000010)	3
				...	...
				63 (111111)	64

The PPULSE field sets the maximum number of IR VCSEL pulses that may occur in a proximity cycle. The proximity engine will automatically continue to add IR VCSEL pulses, up to the value set in PPULSE or if a near-saturation condition occurs if Automatic Pulse Control (APC) is enabled. The dynamic range of the sensor is automatically adjusted to detect distant targets as well as prevent saturation from close targets. This operation also reduces power consumption because proximity integration period is automatically shortened when a target is close to the sensor.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then PPULSE always determines the number of proximity pulses to be transmitted.

PCFG2 Register (Address 0x90)

Figure 30:
PCFG2 Register

Addr: 0x90		PCFG2			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:0	PPULSE_LENL	0x20	RW	These bits are the 8 least significant bits of the 10-bit Pulse Length control setting. The upper 2 bits are in the PCFG1 register. See the PCFG1 register for details. Pulse Length needs to be greater than 16µs.	
				Value	**Pulse Length**
				14 (0000001110)	16µs
				15 (0000001111)	17µs
				Pulse Length = (PPULSE_LEN + 2)µs	
				1023 (1111111111)	1025µs

The PPULSE_LEN, PPULSE and PROX_DATA_AVG together define the VCSEL emitting time within one proximity measurement cycle. The VCSEL works in pulse mode and the working duty cycle needs to be configured less than 5%. The calculation formula for duty cycle is shown below:

Duty Cycle = {(PPULSE_LEN+2)*(PPULSE+1)*(2^PROX_DATA_AVG)} / T_PROX, where the T_PROX is proximity measurement repetition cycle, which is the time length in which the proximity measurement occurs once and updates the PDATA results.

REVID Register (Address 0x91)

Figure 31:
REVID Register

Addr: 0x91		REVID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Reserved	000	R	Reserved
4:3	FUNC_ID	10	R	Device function identification
2:0	REV_ID	001	R	Device revision number

ID Register (Address 0x92)

Figure 32:
ID Register

Addr: 0x92		ID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ID	0x82	R	Device identification

REVID2 Register (Address 0x93)

Figure 33:
REVID2 Register

Addr: 0x93		REVID2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	R	Reserved. Must be set to default value.
3:0	AUX_ID	1101	R	Auxiliary ID

CFG1 Register (Address 0x94)

Figure 34:
CFG1 Register

Addr: 0x94		CFG1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	RW	Reserved. Must be set to default value.
3:1	PD_MUX_SEL	000	RW	This field sets photodiode connection to proximity engine. 000b: The photodiode PROX0 is connected to the proximity engine. 010b: Both photodiodes PROX0 and PROX1 are connected to the proximity engine. All other PD_MUX_SEL values are reserved and should not use.
0	ENAB_TEMP_ SENSOR	0	RW	This field activates temperature sensor. Set PEN =TEN =ENAB_TEMP_SENSOR =1 to enable temperature measurement.

LDR0_CFG Register (Address 0x9A)

Figure 35:
LDR0_CFG Register

Addr: 0x9A		LDR0_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reserved	0	RW	Reserved. Must be set to default value.
6	EN_LDR_0	1	RW	Enables the LDR0.
5:4	ISINK_LSB	01	RW	This field sets VCSEL drive current resolution. **Value** / **VCSEL Drive Current Resolution** 00 / 0.5mA 01 / 1.0mA 10 / 1.5mA 11 / 2.0mA
3:0	PLDRIVE0	0010	RW	This field sets the drive current of the VCSEL driver 0. The formula is shown below: Drive Current 0=(PLDRIVE0+1) x ISINK_LSB. The drive current should be configured within the range of 7mA ~10mA. The values are the nominal current. The actual current through the VCSEL is factory trimmed to normalize the IR intensity.

EYE_SAFETY_CFG Register (Address 0x9E)

Figure 36:
EYE_SAFETY_CFG Register

Addr: 0x9E		EYE_SAFETY_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	EYE_SAFETY_CHKS_ENAB	0	RW	Enables VDD and VSS short check for PLDRIVE0, and also the analog watch dog timer. Eye safety runs only once at the beginning when PON and PEN are enabled.
6	DISABLE_PROX_ON_WD_FAIL	1	RW	Disable the high side switch when the eye safety watch dog expires.
5:0	Reserved	0	RW	Reserved. Must be set to default value.

EYE_SAFETY_STATUS Register (Address 0x9F)

Figure 37:
EYE_SAFETY_STATUS Register

Addr: 0x9F		EYE_SAFETY_STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Reserved	0	R	Reserved. Must be set to default value.
4	EYE_SAFETY_WD_ STATUS_SYNCED	0	R	When the flag is set, it indicates that the watchdog has triggered. When DISABLE_PROX_ON_WD_FAIL is set, the PLDRIVER0 is disabled when this flag is set.
3:2	Reserved	0	R	Reserved. Must be set to default value.
1	PLDRIVE0_PAD_ SHORT_VSS_FAIL	0	R	When the flag is set, it indicates that the VSS check during eye safety check failed for PLDRIVER0. The PLDRIVER0 is disabled (no pulses are sent) in case of failure but the proximity timing is maintained. When ESIEN is 1, an interrupt is generated in the final state after PROX_DATA_AVG is complete. The flag is cleared when PON is made 0. Writing a 1 to this field will clear the flag. To enable clear-by-read function, INT_READ_CLEAR in the register CFG3 must be set to 1.
0	PLDRIVER0_PAD_ SHORT_VDD_FAIL	0	R	When the flag is set, it indicates that the VDD check during eye safety check failed for PLDRIVER0. The PLDRIVER0 is disabled (no pulses are sent) in case of failure but the proximity timing is maintained. When ESIEN is 1, an interrupt is generated in the final state after PROX_DATA_AVG is complete. The flag is cleared when PON is made 0. Writing a 1 to this field will clear the flag. To enable clear-by-read function, INT_READ_CLEAR in the register CFG3 must be set to 1.

STATUS Register (Address 0xA0)

Figure 38:
STATUS Register

Addr: 0xA0		STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PINT_GRT_HTH	0	R, SC	Proximity interrupt is due to PDATA exceeds the high threshold (PIHT). Clearing PINT flag will clear this flag as well.
6	PINT_LES_LTH	0	R, SC	Proximity interrupt is due to PDATA exceeds the low threshold (PILT). Clearing PINT flag will clear this flag as well.
5	PSAT	0	RW, SC	Proximity saturation flag indicates that a PSAT_2STG or AMBCOMP_LVL_SAT or PSAT_1STG_PULSE or PSAT_1STG_AMB event occurred during a previous proximity cycle.
4	PINT	0	RW, SC	Proximity interrupt flag indicates that proximity results have exceeded thresholds and persistence settings.
3	CINT	0	RW, SC	Calibration interrupt flag indicates that calibration has completed.
2	ZINT	0	RW, SC	Zero detection interrupt flag indicates that a zero value in PDATA has caused the proximity offset to be decremented (if PROX_AUTO_OFFSET_ADJUST = 1).
1	PSAT_2STG	0	RW, SC	Proximity saturation interrupt is from second stage of proximity engine.
0	AMBCOMP_LVL_SAT	0	RW, SC	Proximity saturation interrupt is from ambcomp_lvl comparator.

STATUS_2 Register (Address 0xA1)

Figure 39:
STATUS_2 Register

Addr: 0xA1		STATUS_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	VSYNC_LOST	1	R, SC	This flag indicates that VSYNC is not present.
6	POWER_ON_ RESET	1	R, SC	This flag indicates that power on cycle has happened. 0 - No power on reset happened from last read; 1 - Power on reset happened from last read; This flag is clear-by-read by default.

Addr: 0xA1		STATUS_2		
Bit	Bit Name	Default	Access	Bit Description
5	PWINT	0	RW, SC	This flag is set when PWTIME is completed if PWIEN =1. This flag is set only in parallel/concurrent mode and only when PWEN = 1.
4	Reserved	0	RW, SC	Reserved. Must be set to default value.
3	PSAT_1STG_AMB	0	RW, SC	This flag indicates proximity saturation is from first stage of proximity engine due to ambient in subtraction phase.
2	PSAT_1STG_ PULSE	0	RW, SC	This flag indicates proximity saturation is from first stage of proximity engine when VCSEL pulse is emitted.
1	VSYNC_LOST_INT	0	RW, SC	Interrupt when VSYNC watchdog timeout happens or internal oscillator is stopped e.g PON=0. This interrupt generated on event based.
0	VSYNC_CHG_INT	0	RW, SC	Interrupt when there is a change in VSYNC period.

All flags with access type of RW, SC in STATUS and STATUS_2 registers can be cleared by setting the bit high. Alternatively, if the INT_READ_CLEAR in the CFG3 register bit is set, then simply reading this register automatically clears all flags.

CFG2 Register (Address 0xA7)

Figure 40:
CFG2 Register

Addr: 0xA7		CFG2		
Bit	Bit Name	Default	Access	Bit Description
7:2	Reserved	0	RW	Reserved. Must be set to default value.
1	SKIP_IDAC_SAR	1	RW	If set, the IDAC_SAR is skipped.
0	DISABLE_IDAC	1	RW	If set, the IDAC is disabled. If SKIP_IDAC_SAR =DISABLE_IDAC =0, it enables the IDAC to automatically remove most of the ambient IR light to avoid a saturation caused by high ambient IR components. The function runs before every PTIME, and the time required is given by the formula: prox_ init_time =7 x (PPULSE_LEN +42.15µs).

RESET Register (Address 0xA8)

Figure 41:
RESET Register

Addr: 0xA8		RESET		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	RW	Reserved. Must be set to default value.
3	INV_XRES	0	RW	Inverts XRES pin input.
2	ENAB_XRES	0	RW	Enable XRES as a hardware reset pin. By default, level high triggers a device reset.
1	HARD_RESET	0	RW	Perform a POR cycle when this bit is set.
0	SOFT_RESET	0	RW	Software Reset. Writing a '1' triggers a reset of all I^2C registers to default states, including SOFT_RESET bit itself. Due to the reset of PON, a running proximity is aborted and the oscillator is turned off. SOFT_RESET will not set POWER_ON_RESET status bit.

CFG3 Register (Address 0xAB)

Figure 42:
CFG3 Register

<table>
<tr><th colspan="2">Addr: 0xAB</th><th colspan="3">CFG3</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th>Bit Description</th></tr>
<tr><td>7</td><td>INT_READ_CLEAR</td><td>0</td><td>RW</td><td>If set, the interrupt flag bits in the STATUS register will be reset whenever the STATUS register is read over I^2C.</td></tr>
<tr><td>6:5</td><td>MODE_CFG</td><td>10</td><td>RW</td><td>SAI is only available when MODE_CFG = 00b.</td></tr>
<tr><td>4</td><td>SAI</td><td>0</td><td>RW</td><td>The Sleep After Interrupt bit is used to place the device into a low power mode at the end of the proximity cycle if an interrupt has been generated. SAI doesn't modify any register bits directly, it rather uses the interrupt signal to turn off the oscillator. The device will appear as if PON=0, however, PON will read as 1. The way to wake up the device from SAI-sleep is by clearing the interrupts in the status registers. Note that SAI is only available when MODE_CFG = 00b.
<table>
<tr><th>PON</th><th>SAI</th><th>INT (low active)</th><th>Oscillator</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>OFF</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>ON</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>ON</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>OFF</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>Reserved</td><td>0001</td><td>RW</td><td>Reserved. Must be set to default value.</td></tr>
</table>

CFG6 Register (Address 0xAE)

Figure 43:
CFG6 Register

Addr: 0xAE		CFG6		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reserved	0	RW	Reserved. Must be set to default value.
6	DISABLE_APC	1	RW	Proximity automatic pulse control (APC) disable. 0 = APC enable; 1 = APC disable; This bit should be set to 1 when calibration needs to be performed.
5:0	Reserved	111111	RW	Reserved. Must be set to default value.

VSYNC_CFG Register (Address 0xB1)

Figure 44:
VSYNC_CFG Register

Addr: 0xB1		VSYNC_CFG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:6	Reserved	00	RW	Reserved. Must be set to default value.	
5:4	VSYNC_CHG_ DET_STP	00	RW	VSYNC period change detection step. Once VSYNC period changes from previous cycle by step of period mentioned in the following table, VSYNC_CHG_INT interrupt is generated if VSIEN=1. VSYNC_PRD ={VSYNC_PRD_H, VSYNC_PRD_L}	
				Value	**Timing**
				0	Compare with VSYNC_PRD[15:10]
				1	Compare with VSYNC_PRD[15:9]
				2	Compare with VSYNC_PRD[15:11]
				3	Compare with VSYNC_PRD[15:12]
3	INT_VSYNC_EN	0	RW	Enables internal VSYNC. It will be cleared automatically when VSYNC signal is detected on the device VSYNC pin.	
2	VSYNC_INVERT	0	RW	This bit inverts VSYNC input. 0 – Not inverted; 1 – Inverted;	
1:0	VSYNC_WD_TH	0	RW	VSYNC watch dog time out. The expiration generates VSYNC_LOST_INT interrupt if VSIEN=1.	
				Value	**Timing**
				0	88.92ms
				1	11.12ms
				2	22.23ms
				3	44.46ms

VSYNC_PRD_L Register (Address 0xB2)

Figure 45:
VSYNC_PRD_L Register

Addr: 0xB2		VSYNC_PRD_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	VSYNC_PRD_L	0x00	RW	The low byte of the 16-bit VSYNC period data.

VSYNC_PRD_H Register (Address 0xB3)

Figure 46:
VSYNC_PRD_H Register

Addr: 0xB3		VSYNC_PRD_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	VSYNC_PRD_H	0x00	RW	The high byte of the 16-bit VSYNC period data.

VSYNC_PRD stores the last VSYNC signal period. This is 16-bit divided into 2 registers {VSYNC_PRD_H, VSYNC_PRD_L} with resolution of 1.357µs/bit. It is recommended that VSYNC signal is in the frequency range of 11.25Hz to 1KHz with minimum active pulse width 16µs, although the counter is able to detect a much higher frequency. Once external VSYNC signal is lost, VSYNC_LOST_INT interrupt is generated if VSIEN =1. Then software has option to enable internal VSYNC by enabling INT_VSYNC_EN. The internal VSYNC will generate with frequency of last period stored in VSYNC_PRD registers. Users can write VSYNC_PRD registers for a desired frequency before enabling the internal VSYNC feature. Once the device detects external VSYNC signal, the INT_VSYNC_EN bit will be cleared automatically, VSYNC_PRD value will update according to the period detected.

POFFSET Register (Address 0xC0)

Figure 47:
POFFSET Register

Addr: 0xC0		POFFSET		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	POFFSET	0x00	RW	This register contains the magnitude portion of proximity offset adjust value.

POFFSET_SIGN Register (Address 0xC1)

Figure 48:
POFFSET_SIGN Register

Addr: 0xC1		POFFSET_SIGN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Reserved	0000000	RW	Reserved. Must be set to default value.
0	POFFSET_ SIGN	0	RW	This register contains the sign portion of proximity offset adjust value.

Typically, optical and/or electrical crosstalk negatively influence proximity operation and results. The POFFSET /POFFSET_SIGN registers provide a mechanism to remove system crosstalk from the proximity data. POFFSET /POFFSET_ SIGN contains the magnitude and sign of a value that adjusts PDATA in the AFE. An offset value in the range of ± 255 is possible.

CALIB Register (Address 0xD7)

Figure 49:
CALIB Register

Addr: 0xD7		CALIB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	OFFCAL_ENAB_AVG	0	RW	Enables proximity hardware averaging as selected with PROX_DATA_AVG during calibration. 0 = No hardware averaging; 1 = Hardware averaging enabled.
6	Reserved	0	RW	Reserved. Must be set to default value.
5	ELECTRICAL_ CALIBRATION	0	RW	Selects proximity calibration type. 0 = Electrical and optical crosstalk; 1 = Electrical crosstalk only.
4	PTIME_IN_CALIB	0	RW	Enables PTIME during calibration. Useful when averaging is enabled. 0 = PTIME ignored during calibration; 1 = PTIME enabled during calibration.
3:1	Reserved	000	RW	Reserved. Must be set to default value.
0	START_OFFSET_CAL	0	RW	Set to 1 to start a calibration sequence.

Proximity response in systems with electrical and optical crosstalk may be improved by using the calibration feature. Optical crosstalk is caused when the photodiode receives a portion of the VCSEL IR, which was unintentionally reflected by a surface other than the target. Electrical offset is caused by electrical disturbance in the sensor AFE, and influences the proximity result as well. Before starting the calibration, it is required to set PEN, AEN and PON to 0 to bring the state machine idle, and set DISABLE_APC to 1 to disable the auto pulse control. The calibration target, BINSRCH_TARGET, needs to be configured to a desired value, the calibration routine adjusts the value in POFFSET /POFFSET_SIGN until the proximity result is as close to the BINSRCH_TARGET as possible.

The calibration needs to run with the same settings as regular proximity measurement, such as PPULSE, PPULSE_LEN, PGAIN, PGAIN2, PLDRIVE0. If PTIME_IN_CALIB is enabled, the same PTIME used for regular proximity measurement is also enabled during the calibration. If OFFCAL_ENAB_AVG is enabled, the hardware averaging as selected with PROX_DATA_AVG is enabled as well during the calibration. The calibration needs to run 9 proximity measurement cycles. If every cycle of the 9 cycles needs to be synchronized to the VSYNC signal with PSD delay, PROX_CAL_VSYNC_EN has to be enabled. After all the settings properly configured, PON needs to be enabled again

in order to run the calibration successfully. An electrical calibration can be initiated at any time by setting the ELECTRICAL_CALIBRATION and START_OFFSET_CAL bits. To perform an optical (and electrical) calibration do not set the ELECTRICAL_CALIBRATION bit when setting the START_OFFSET_CAL bit. Electrical and optical calibration functions are identical, except that during an electrical calibration the proximity photodiode is disconnected from the AFE.

Upon completion of the calibration, proximity offset registers are automatically loaded with calibration result, START_OFFSET_CAL bit will be self-cleared, the CINT flag will assert. If CIEN is enabled, an interrupt is generated on the INT pin.

CALIB_OFFSET Register (Address 0xD8)

Figure 50:
CALIB_OFFSET Register

Addr: 0xD8		CALIB_OFFSET			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	Reserved	0	RW	Reserved. Must be set to default value.	
6	EN_AUTO_ ORE_CAL	0	RW	Setting this bit to a 1 enables automatic calculation for PRX_OFFSET_RANGE_EXTENSION during proximity calibration. When the bit is 0, the automatic calculation is disabled, and the PRX_OFFSET_RANGE_EXTENSION value has to be provided by users.	
5	EN_PRX_ OFFSET_ RANGE_ EXTENSION	0	RW	Setting this bit to a 1 enables the proximity offset range extension functionality. See the PRX_OFFSET_ RANGE_EXTENSION bits. If this bit is set to 0, the offset range extension is disabled.	
4:0	PRX_OFFSET_ RANGE_ EXTENSION	00000	RW	Offset range extension selection. For PGAIN2 = 2.5x, all 5 bits are used. For PGAIN2 = 5x, the LSB is ignored. For PGAIN2 = 10x, 2 LSBs are ignored.	
				Value	**Selection**
				0 (00000)	Nominal
				1 (00001)	Nominal + 1 Step
				2 (00010)	Nominal + 2 Steps
				3 (00011)	Nominal + 3 Steps
				Nominal + (Value) Steps	
				31 (11111)	Nominal + 31 Steps

For applications with high optical proximity crosstalk (the emitted IR optical signal appears at the IR sensor), the offset range can be extended in discrete steps. To determine the best range extension step for the application, a proximity calibration cycle is initiated and the resulting proximity offset is captured in the POFFSET /POFFSET_SIGN registers.

CALIBCFG Register (Address 0xD9)

Figure 51:
CALIBCFG Register

Addr: 0xD9		CALIBCFG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	BINSRCH_ TARGET	010	RW	Proximity offset calibration result target.	
				Value	**PDATA Target**
				0 (000)	3
				1 (001)	7
				2 (010)	15
				3 (011)	31
				4 (100)	63
				5 (101)	127
				6 (110)	255
				7 (111)	511
4	Reserved	1	RW	Reserved. Must be set to default value.	
3	PROX_AUTO_ OFFSET_ ADJUST	0	RW	If set, then in proximity mode, whenever an ADC measurement yield zero, the pertinent offset register will be decreased. Will set the OFFSET_ADJUSTED flag if it happened. Note that if a diode is disabled, this mechanism is disabled as well.	
2:0	PROX_DATA_ AVG	0 (000)	RW	PROX_DATA_AVG defines the number of ADC samples collected and hardware averaged during a proximity cycle.	
				Value	**Sample Size**
				0 (000)	Disable
				1 (001)	2
				2 (010)	4
				3 (011)	8
				4 (100)	16
				All other values	Reserved

The BINSRCH_TARGET field is used by the calibration feature to set the baseline value for PDATA when no target is present. For example, calibration of a device in open air, with no target, and

BINSRCH_TARGET setting of 2 causes the PDATA value will be approximately 15 counts. This feature is useful because it forces PDATA result to always be above zero.

The PROX_DATA_AVG field sets the number of ADC samples that are averaged. Each ADC sample causes the programmed number of proximity pulses to be transmitted. Once all samples have been completed and the average is calculated, the proximity state machine will then pass this value either directly to PDATA.

PCFG4 Register (Address 0xDA)

Figure 52:
PCFG4 Register

Addr: 0xDA		PCFG4		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Reserved	0	RW	Reserved. Must be set to default value.
0	PROX_CAL_ VSYNC_EN	0	RW	The bit enables proximity calibration synchronized to the VSYNC signal with PSD delay. The proximity calibration consists of 9 measurement cycles. If the bit is set to 1, every cycle of the 9 measurement cycles are synchronized to the VSYNC signal with PSD delay. If the bit is set to 0 and PVSYNC_EN is 1, only the first measurement cycle is synchronized to the VSYNC signal with PSD delay, the successive measurement cycles run immediately after the first measurement cycle. If the bit is set to 0 and PVSYNC_EN is 0, all 9 measurement cycles of the proximity calibration run immediately pulse burst irrespective of VSYNC signal.

CALIBSTAT Register (Address 0xDC)

Figure 53:
CALIBSTAT Register

Addr: 0xDC		CALIBSTAT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	00000	R	Reserved. Must be set to default value.
2	OFFSET_ ADJUSTED	0	R	Bit is set when the proximity offset has been automatically decremented if PROX_AUTO_ OFFSET_ADJ = 1 (see CALIBCFG register). This bit can be cleared by writing 1 to it or setting PROX_AUTO_OFFSET_ADJ to 0.

Addr: 0xDC		CALIBSTAT		
Bit	Bit Name	Default	Access	Bit Description
1	Reserved	0	R	Reserved. Must be set to default value.
0	CALIB_FINISHED	0	R	This flag indicates that calibration has finished. This bit is a copy of the CINT bit in the STATUS register. It will be cleared when the CINT bit is cleared.

INTENAB Register (Address 0xDD)

Figure 54:
INTENAB Register

Addr: 0xDD		INTENAB		
Bit	Bit Name	Default	Access	Bit Description
7	Reserved	0	RW	Reserved. Must be set to default value.
6	PSIEN	0	RW	Proximity Saturation Interrupt Enable.
5	PIEN	0	RW	Proximity Interrupt Enable.
4	Reserved	0	RW	Reserved. Must be set to default value.
3	CIEN	0	RW	Calibration Interrupt Enable.
2	ZIEN	0	RW	Zero Detect Interrupt Enable.
1	HYS_PIEN	0	RW	1 = Enables hysteresis based proximity interrupt; 0 = Enables level based proximity interrupt.
0	VSIEN	0	RW	VSYNC related interrupt enable.

INTENAB_2 Register (Address 0xDE)

Figure 55:
INTENAB_2 Register

Addr: 0xDE		INTENAB_2		
Bit	Bit Name	Default	Access	Bit Description
7:5	Reserved	000	RW	Reserved. Must be set to default value.
4	ESIEN	0	RW	Eye safety failure interrupt enable.
3:2	Reserved	00	RW	Reserved. Must be set to default value.
1	PWIEN	0	RW	PWTIME completion interrupt enable.
0	Reserved	0	RW	Reserved. Must be set to default value.

PSD_L Register (Address 0xEA)

Figure 56:
PSD_L Register

Addr: 0xEA		PSD_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PSD_L	0x00	RW	This is lower byte of Proximity Start Delay time. It's 16-bit value split into 2 registers {PSD_H[7:0],PSD_L[7:0]}. It is in multiples of 1.357µs.

Value	Delay Cycles	Delay Time
0x0000	0	Disabled
0x0001	1	1.357µsx1
0x0002	2	1.357µsx2
…	…	…
0x3FFF	16383	1.357µsx16383
…	…	…
0xFFFF	65535	1.357µsx65535

PSD_H Register (Address 0xEB)

Figure 57:
PSD_H Register

Addr: 0xEB		PSD_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PSD_H	0x00	RW	This is upper byte of Proximity Start Delay time. See PSD_L for details.

The PSD (Proximity Start Delay) timing registers control the start of proximity measurement after detect of VSYNC signal. It is a 16-bit value split into two registers {PSD_H [7:0], PSD_L [7:0]}. PSD needs to be programmed less than VSYNC period, since the counter will reset once VSYNC signal is detected. If VSYNC is changed, PSD period and other configurations need to be changed accordingly by bringing device in IDLE mode by stopping integration.

PWTIME Register (Address 0xEC)

Figure 58:
PWTIME Register

Addr: 0xEC		PWTIME				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**		
7:0	PWTIME	0x00	RW	Value that specifies the proximity wait time in 2.779ms increments.		
				Value	**Wait Cycles**	**Wait Time**
				0x00	1	2.779ms (33.346ms)
				0x01	2	5.558ms (66.692ms)
				0x02	3	8.336ms (100.038ms)
				…	…	…
				0x1F	32	88.923ms (1.067s)
				…	…	…
				0xFF	256	711.381ms (8.537s)

The PWTIME is implemented using a down counter and starts counting from very beginning of every proximity measurement cycle including the initialization time. If enabled, PWTIME needs to be programmed greater than proximity measurement time, otherwise it's ignored.

PWTIME =Wait Cycles x2.779ms.

If PWLONG is enabled, then PWTIME =Wait Cycles x2.779ms x12.

Note that PWTIME is ignored if MODE_CFG (CFG3 (0xAB), bit[6:5])=00b.

PDATA_L Register (Address 0xF4)

Figure 59:
PDATA_L Register

Addr: 0xF4		PDATA_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PDATA_L	0x00	R	If APC is enabled, this register contains the low byte of the 14-bit proximity data. If APC is disabled, this register contains the upper 8 most significant bits of the 10-bit proximity data.

PDATA_H Register (Address 0xF5)

Figure 60:
PDATA_H Register

Addr: 0xF5		PDATA_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PDATA_H	0x00	R	If APC is enabled, this register contains the high byte of the 14-bit proximity data. If APC is disabled, bits 1:0 contain the lower 2 bits of the 10-bit proximity value.

Proximity detection uses an Automatic Pulse Control (APC) mechanism that adjusts the number of pulses per measurement based on the magnitude of the reflected IR signal. As the magnitude of the signal increases, the number of pulses decreases.

Dependent on the configurations, proximity data can be stored as a 10-bit, 14-bit, or 16-bit value (two bytes). Reading the low byte first latches the high byte.

When Automatic Pulse Control (APC) is enabled by setting DISABLE_APC=0 (bit6 of CFG6), proximity detection uses a 10-bit ADC that is extended to a 14-bit or 16-bit dynamic range for PDATA.

If ENAB_16_BIT_OP =0, PDATA is a 14-bit value, PDATA = ADCvalue x (16 / actual number of pulses transmitted);

If ENAB_16_BIT_OP =1, PDATA is a 16-bit value, PDATA = ADCvalue x (64 / actual number of pulses transmitted);

PDATA is therefore proportional to the reflected energy independent of the number of pulses transmitted.

When Automatic Pulse Control (APC) is disabled by setting DISABLE_APC=1 (bit6 of CFG6), then the proximity data converts to a 10-bit value. PDATAL contains the 8 most significant bits of the 10-bit value and PDATAH bit locations 1:0 contain the lower 2-bits. When APC is disabled, only the upper 8-bits are compared against the threshold values contained in PILTL and PIHTL.

TDATA_L Register (Address 0xF6)

Figure 61:
TDATA_L Register

Addr: 0xF6		TDATA_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	TDATA_L	0x00	R	Temperature ADC data LSB[7:0] Temperature data is stored as a 10-bit value split into two registers. Once PEN =TEN =ENAB_TEMP_SENSOR =1, temperature measurement is activated, and TDATA is updated automatically after every proximity measurement. T(ºC)=(399-TDATA)/1.48

TDATA_H Register (Address 0xF7)

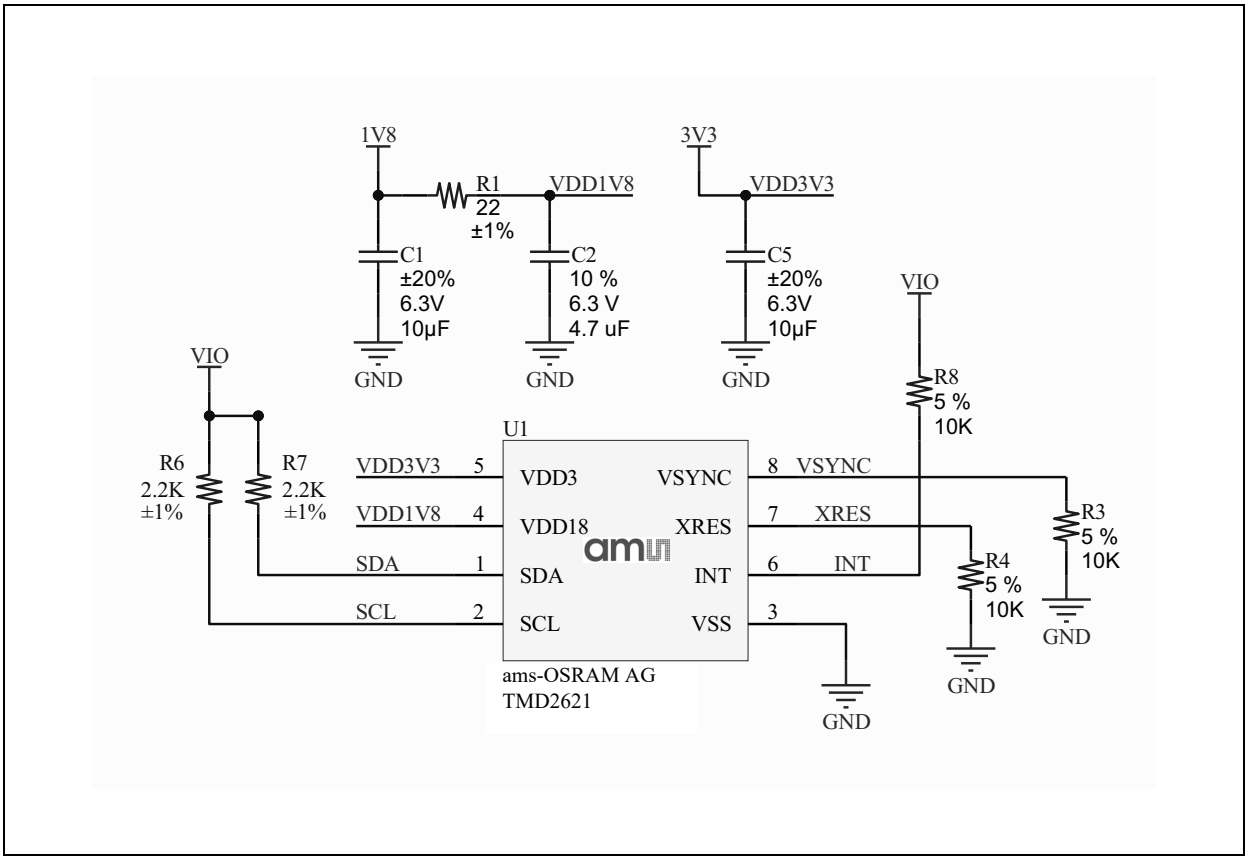
Figure 62:
TDATA_H Register

Addr: 0xF7		TDATA_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	TDATA_H	0x00	R	Temperature ADC data MSB[9:8] See TDATA_L for details.

Application Information

Schematic

Figure 63:
TMD2621 Typical Application Circuit

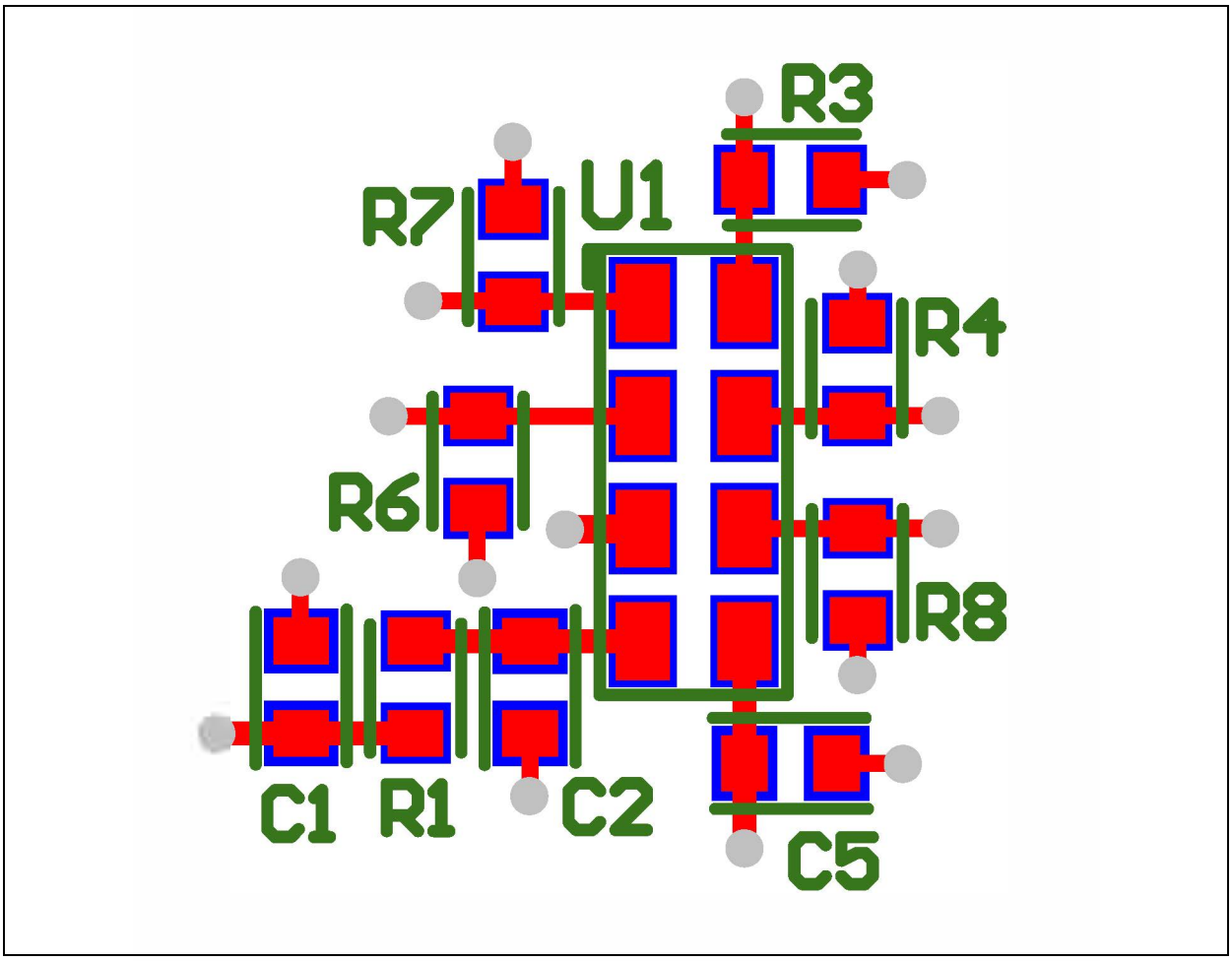


Note(s):

1. Place VDD18 filter (R1, C1, C2) and VDD3 filter (C5) as close as possible to the module.
2. The value of the I^2C pull up resistors (R6, R7) should be based on the bus voltage, system bus speed and trace capacitance.
3. R1, C1, C2, C5 are critical components to protect the device during high voltage ESD strikes.
4. In systems subjected to high voltage ESD strikes, it is recommended to connect XRES to a host GPIO pin to allow the device reset.

Recommended Circuit Layout

Figure 64:
TMD2621 Recommended Circuit Layout

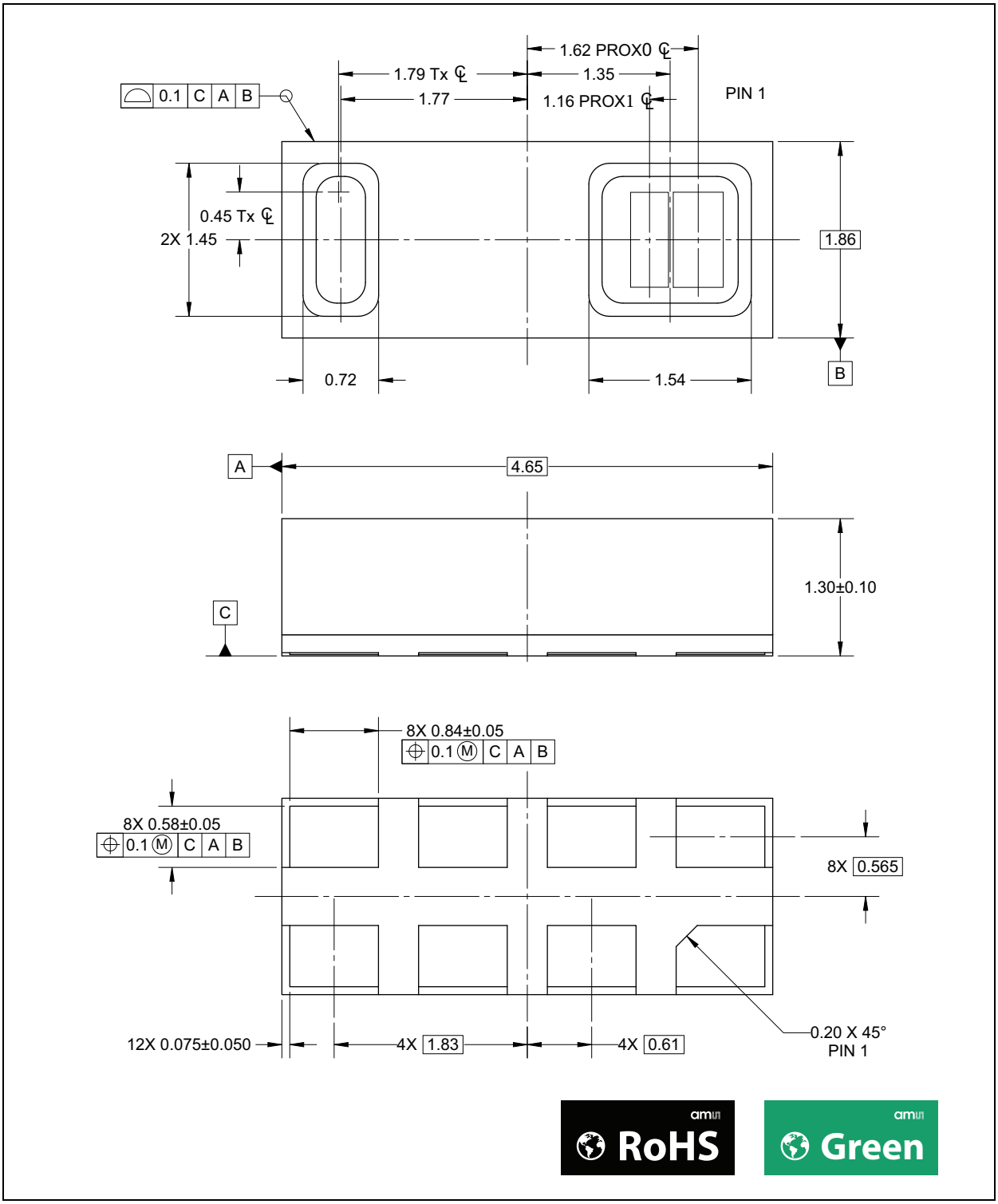


Note(s):

1. The placement of the decoupling capacitors are critical. Place the components on the same side of PCB as device as shown in the figure above. Make connections as close as possible to minimize series inductance and resistance.

Package Drawings & Markings

Figure 65:
TMD2621 Package Drawings



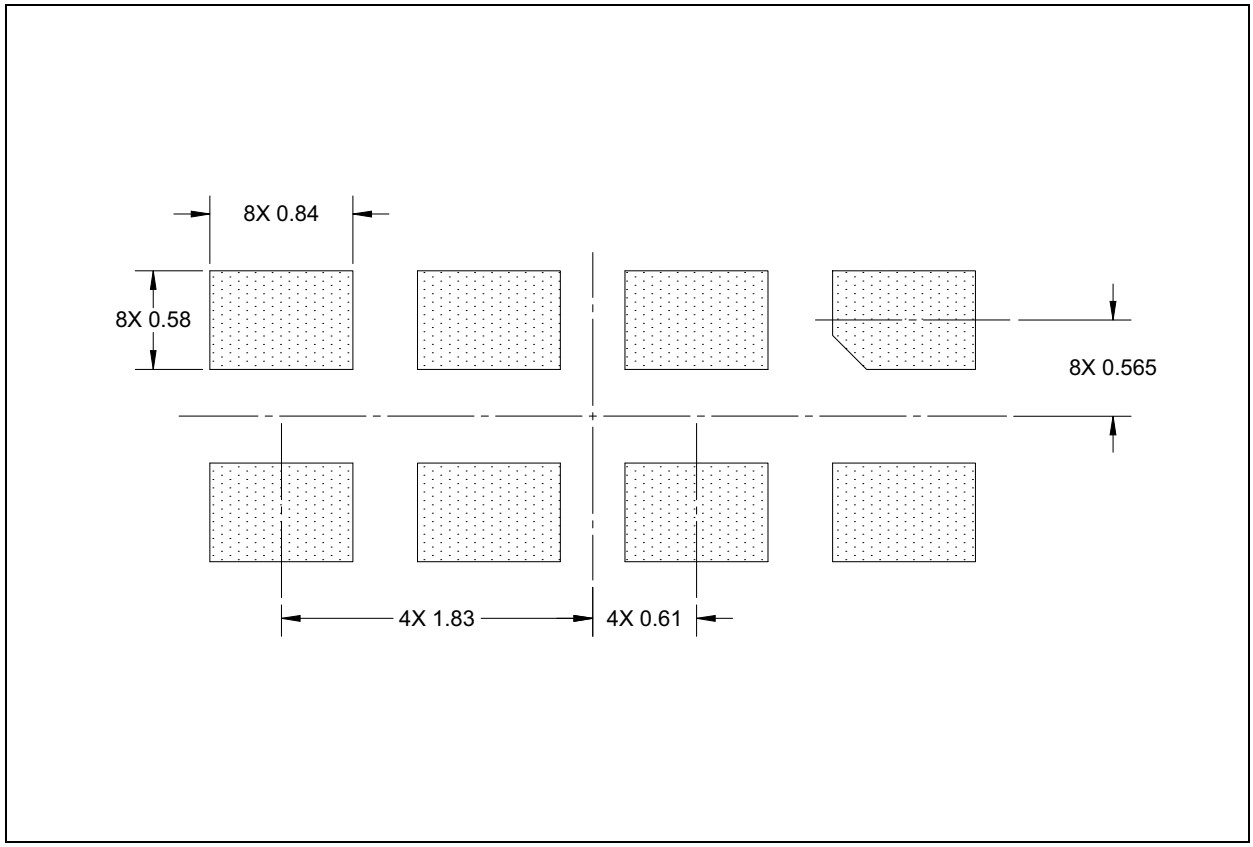
Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerances are ±0.05mm unless otherwise noted.
3. Contact finish is Au.
4. This package contains no lead (Pb).
5. This drawing is subject to change without notice.

Recommended PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads.

Figure 66:
Recommended PCB Pad Layout

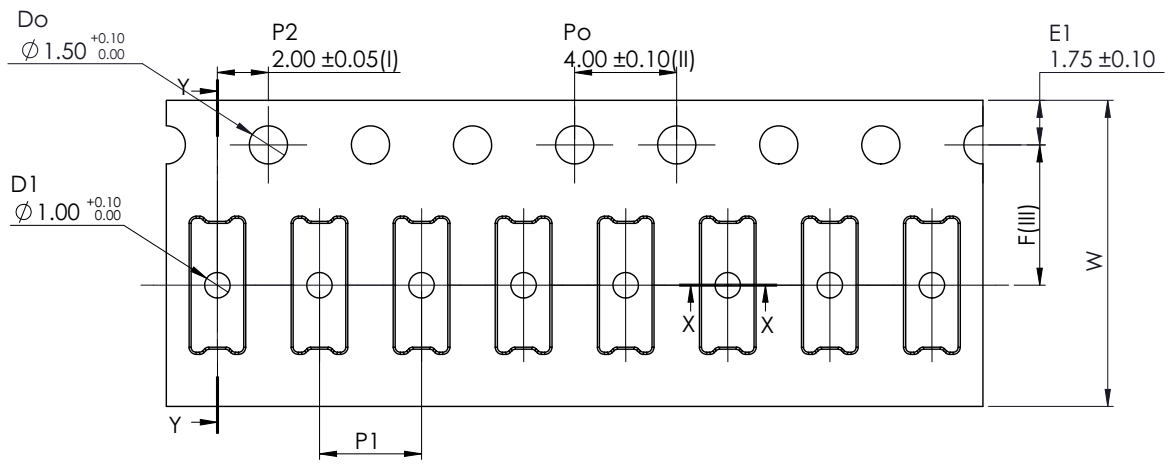


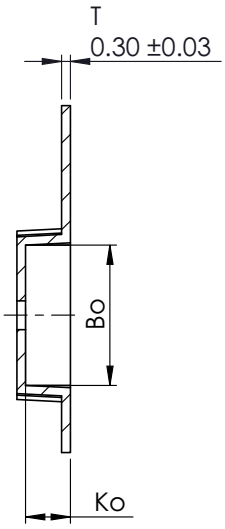
Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerances are 0.05mm unless otherwise noted.
3. This drawing is subject to change without notice.

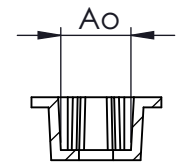
Tape & Reel Information

Figure 67:
TMD2621 Tape and Reel Information

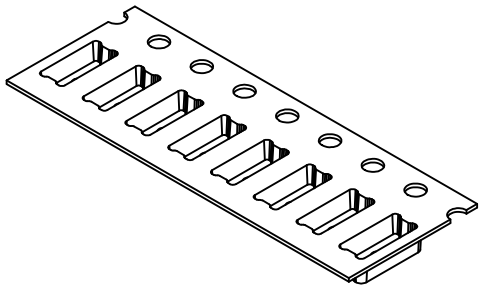




SECTION Y-Y



SECTION X-X



Ao	2.06	+/- 0.05
Bo	4.85	+/- 0.05
Ko	1.55	+/- 0.10
F	5.50	+/- 0.05
P1	4.00	+/- 0.10
W	12.00	+0.30/-0.10

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20.
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Dimension with ( ) is used for design reference purposes No measurement required.

Note(s):

1. All linear dimensions are in millimeters unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing Ao, Bo, and Ko are defined in ANSI EIA Standard 481-B 2001
4. ams OSRAM packaging tape and reel conform to the requirements of EIA Standard 481-B.
5. In accordance with EIA standard device pin 1 is located next to the sprocket holes in the tape.
6. This drawing is subject to change without notice.

Soldering & Storage Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

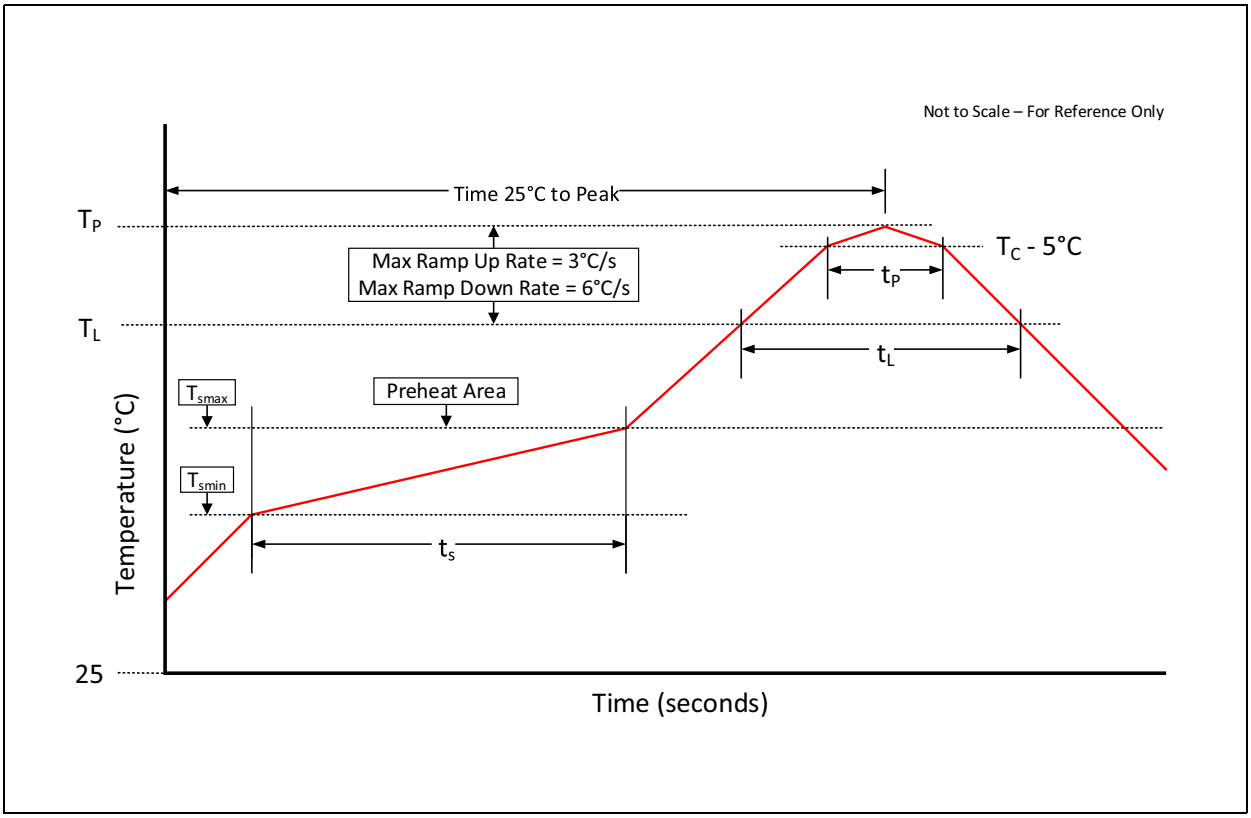
Figure 68:
Solder Reflow Profile

Profile Feature Preheat/ Soak	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Temperature Min (T_{smin})	100 °C	150 °C
Temperature Max (T_{smax})	150 °C	200 °C
Time (t_s) from (T_{smin} to T_{smax})	60s - 120s	60s -120s
Ramp-up rate (T_L to T_P)	3 °C/s max.	3 °C/s max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60s - 150s	217 °C 60s - 150s
Peak package body temperature (T_P)	For users T_P must not exceed the classification temp. of 235 °C. For suppliers T_P must equal or exceed the classification temp. of 235 °C.	For users T_P must not exceed the classification temp. of 260 °C. For suppliers T_P must equal or exceed the classification temp. of 260 °C.
Time (t_P)[(1)] within 5 °C of the specified classification temperature (T_c)	20[(1)]s	30[(1)]s
Ramp-down rate (T_P to T_L)	6 °C/s max.	6 °C/s max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note(s):

1. Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum.

Figure 69:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 24 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 24 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 24 months shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

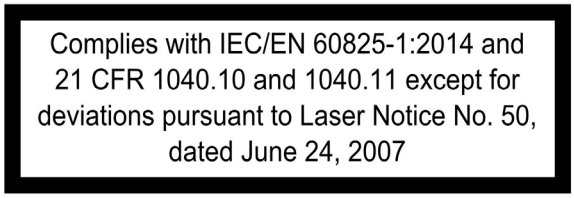
- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Laser Eye Safety



The TMD2621 is designed to meet the Class 1 laser safety limits including single faults in compliance with IEC/EN 60825-1:2014. In an end application system environment, the system may need to be tested to ensure it remains compliant. The system must not include any additional lens to concentrate the laser light or parameters set outside of the recommended operating conditions or any physical modification to the module during development could result in hazardous levels of radiation exposure.

Ordering & Contact Information

Figure 70:
Ordering Information

Ordering Code	I²C Bus	I²C Address	Delivery Form	Delivery Quantity
TMD26213	1.8V	0x39	Tape & Reel (13”)	10000 pcs/reel
TMD26213M	1.8V	0x39	Tape & Reel (7”)	1000 pcs/reel

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

Changes from 3-00 (2022-Sep-16) to current revision 4-00 (2023-Apr-12)	Page
Updated the document security class from “Confidential” to “Public”	
Added the I^2C Timing Characteristics	11
Updated “Shelf Life” to 24 months	50
Updated the Delivery Quantity from 2500pcs/reel to 1000pcs/reel for TMD26213M	52

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide