Suggested Board Reflow Profile

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Reference</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average temperature gradient in preheating</td>
<td></td>
<td>2.5 °C/sec</td>
</tr>
<tr>
<td>Soak time</td>
<td>t_soak</td>
<td>2 to 3 minutes</td>
</tr>
<tr>
<td>Time above 217 °C (T1)</td>
<td>t_1</td>
<td>Max 60 sec</td>
</tr>
<tr>
<td>Time above 230 °C (T2)</td>
<td>t_2</td>
<td>Max 50 sec</td>
</tr>
<tr>
<td>Time above T_peak - 10 °C (T3)</td>
<td>t_3</td>
<td>Max 10 sec</td>
</tr>
<tr>
<td>Peak temperature in reflow</td>
<td>T_peak</td>
<td>260 °C</td>
</tr>
<tr>
<td>Temperature gradient in cooling</td>
<td></td>
<td>Max -5 °C/sec</td>
</tr>
</tbody>
</table>

TMF8701 Daughter Card

Revision History

Version: A  J.Dolic
Initial Release
Either Place U1 or U2, but not both
Board Details
1. Board Size: 750mil x 1250mil +/- 10%
2. Board Thickness: 62mil +/- 10%
3. Board material: FR4 with 0.5oz Copper
4. Component count: 25
5. Pad Count: 80
6. Hole Count: 43
7. Soldermask Color: Black
8. Silkscreen Color: White
9. No Silkscreen over exposed copper.
10. PCB Manufacturer not to add any additional silkscreen
11. Fabricate to IPC-600 Class 1 unless otherwise specified
12. RoHS compliant
13. There are two score marks on this board.

Layers Currently On

Title_Block
Top Layer

BoardOutline

Title TMF8701 Daughter Card
Number DC-TMF8701-01
Rev B
Print Name DC-TMF8701-01

Variant: [No Variations] Print Date: 20.03.2019
File: PCB_PcbDoc Drawn By: J.Dollc
**Board Details**

1. Board Size: 750mil x 1250mil +/- 10%
2. Board Thickness: 62mil +/- 10%
3. Board material: FR4 with 0.5oz Copper
4. Component count: 25
5. Pad Count: 80
6. Hole Count: 43
7. Soldermask Color: Black
8. Silkscreen Color: White
9. No Silkscreen over exposed copper.
10. PCB Manufacturer not to add any additional silkscreen
11. Fabricate to IPC-600 Class 1 unless otherwise specified
12. RoHS compliant
13. There are two score marks on this board.

**Layers Currently On**

- Title_Block
- MID1
- BoardOutline

---

**Title**

TMF8701 Daughter Card

**Number**

DC-TMF8701-01

**Rev**

B

**Print Name**

Mid1 Layer - GND

---

**File**

PCB_PcbDoc

**Drawn By**

J.Dollic

---

**Print Date**

20.03.2019
Board Details
1. Board Size: 750mil x 1250mil +/- 10%
2. Board Thickness: 62mil +/- 10%
3. Board material: FR4 with 0.5oz Copper
4. Component count: 25
5. Pad Count: 80
6. Hole Count: 43
7. Soldermask Color: Black
8. Silkscreen Color: White
9. No Silkscreen over exposed copper.
10. PCB Manufacturer not to add any additional silkscreen
11. Fabricate to IPC-600 Class 1 unless otherwise specified
12. RoHS compliant
13. There are two score marks on this board.

Layers Currently On

Title_Block

MID2

BoardOutline

Multi-Layer
Board Details
1. Board Size: 750mil x 1250mil +/- 10%
2. Board Thickness: 62mil +/- 10%
3. Board material: FR4 with 0.5oz Copper
4. Component count: 25
5. Pad Count: 80
6. Hole Count: 43
7. Soldermask Color: Black
8. Silkscreen Color: White
9. No Silkscreen over exposed copper.
10. PCB Manufacturer not to add any additional silkscreen
11. Fabricate to IPC-600 Class 1 unless otherwise specified
12. RoHS compliant
13. There are two score marks on this board.

Layers Currently On
Title_Block
Bottom Layer
BoardOutline
Bottom Overlay
Multi-Layer
Board Details
1. Board Size: 750mil x 1250mil +/- 10%
2. Board Thickness: 62mil +/- 10%
3. Board material: FR4 with 0.5oz Copper
4. Component count: 25
5. Pad Count: 80
6. Hole Count: 43
7. Soldermask Color: Black
8. Silkscreen Color: White
9. No Silkscreen over exposed copper.
10. PCB Manufacturer not to add any additional silkscreen
11. Fabricate to IPC-600 Class 1 unless otherwise specified
12. RoHS compliant
13. There are two score marks on this board.

Layers Currently On
- Title_Block
- Dimension
- BoardOutline
- Drill Guide
- Keep-Out Layer
- Multi-Layer

Title TMF8701 Daughter Card
Number DC-TMF8701-01
Rev B
Print Name
Board Dimensions
Variant: (No Variations)
Board Details
1. Board Size: 750mil x 1250mil +/- 10%
2. Board Thickness: 62mil +/- 10%
3. Board material: FR4 with 0.5oz Copper
4. Component count: 25
5. Pad Count: 80
6. Hole Count: 43
7. Soldermask Color: Black
8. Silkscreen Color: White
9. No Silkscreen over exposed copper.
10. PCB Manufacturer not to add any additional silkscreen
11. Fabricate to IPC-600 Class 1 unless otherwise specified
12. RoHS compliant
13. There are two score marks on this board.

Layers Currently On

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Count</th>
<th>Hole Size</th>
<th>Plated</th>
<th>Hole Type</th>
<th>Drill Layer</th>
<th>Pad</th>
<th>Pad Shape</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2</td>
<td>100,000mil (2,540mm)</td>
<td>NPTH</td>
<td>Round</td>
<td>TOP - BOTTOM</td>
<td>Pad</td>
<td>Rounded</td>
<td>±0.05mm254</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>100,000mil (2,540mm)</td>
<td>PTH</td>
<td>Round</td>
<td>TOP - BOTTOM</td>
<td>Pad</td>
<td>Rounded</td>
<td>±0.20mm±0.035±0.25</td>
</tr>
<tr>
<td>□</td>
<td>37</td>
<td>8.00mil (0.203mm)</td>
<td>DPTH</td>
<td>Round</td>
<td>TOP - BOTTOM</td>
<td>Use</td>
<td>Rounded</td>
<td>V46±20</td>
</tr>
</tbody>
</table>

43 Total
Board Details
1. Board Size: 750mil x 1250mil +/- 10%
2. Board Thickness: 62mil +/- 10%
3. Board material: FR4 with 0.5oz Copper
4. Component count: 25
5. Pad Count: 80
6. Hole Count: 43
7. Soldermask Color: Black
8. Silkscreen Color: White
9. No Silkscreen over exposed copper.
10. PCB Manufacturer not to add any additional silkscreen
11. Fabricate to IPC-600 Class 1 unless otherwise specified
12. RoHS compliant
13. There are two score marks on this board.

Layers Currently On
Title_Block
BoardOutline
TopAssembly
Multi-Layer

Title  TMF8701 Daughter Card
Number DC-TMF8701-01  Rev B
Print Name TOP Assembly
Variant: [No Variations]  Print Date: 20.03.2019
File: PGS.PcbDoc  Drawn By: J.Oldic
Board Details
1. Board Size: 750mil x 1250mil +/- 10%
2. Board Thickness: 62mil +/- 10%
3. Board material: FR4 with 0.5oz Copper
4. Component count: 25
5. Pad Count: 80
6. Hole Count: 43
7. Soldermask Color: Black
8. Silkscreen Color: White
9. No Silkscreen over exposed copper.
10. PCB Manufacturer not to add any additional silkscreen.
11. Fabricate to IPC-600 Class 1 unless otherwise specified.
12. RoHS compliant
13. There are two score marks on this board.

Layers Currently On
- Title_Block
- BoardOutline
- BottomAssembly
- Multi-Layer

Title TMF8701 Daughter Card
Number DC-TMF8701-01
Rev B
Print Name BOTTOM Assembly Mirrored
Variant: [No Variations] Print Date: 20.03.2019
File: PCB.ProDoC Drawn By: J.Ollec
## Design Rules Verification Report

**Filename:** `\fsup04\cnc_prodmgmt\OSL\11_HW_Application_PS\Koloth\Hardware\DC-Dual_T`

### Warnings

<table>
<thead>
<tr>
<th>Warning</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clearance Constraint (Gap=5mil) (All),(All)</td>
<td>0</td>
</tr>
<tr>
<td>Short-Circuit Constraint (Allowed=No) (All),(All)</td>
<td>0</td>
</tr>
<tr>
<td>Short-Circuit Constraint (Allowed=Yes) (IsTextInverted),(All)</td>
<td>0</td>
</tr>
<tr>
<td>Un-Routed Net Constraint ( (All) )</td>
<td>0</td>
</tr>
<tr>
<td>Width Constraint (Min=4.921mil) (Max=393.701mil) (Preferred=11.811mil) (All)</td>
<td>0</td>
</tr>
<tr>
<td>Power Plane Connect Rule(Relief Connect ) (Expansion=15.748mil) (Conductor Width=5.906mil) (Air Gap=5.906mil)</td>
<td>0</td>
</tr>
<tr>
<td>Minimum Annular Ring (Minimum=5mil) (All)</td>
<td>0</td>
</tr>
<tr>
<td>Hole Size Constraint (Min=6mil) (Max=232.284mil) (All)</td>
<td>0</td>
</tr>
<tr>
<td>Hole To Hole Clearance (Gap=11.811mil) (All),(All)</td>
<td>0</td>
</tr>
<tr>
<td>Minimum Solder Mask Silver (Gap=1mil) (All),(All)</td>
<td>0</td>
</tr>
<tr>
<td>Silk To Solder Mask (Clearance=0mil) (IsPad),(All)</td>
<td>0</td>
</tr>
<tr>
<td>Silk to Silk (Clearance=0mil) (All),(All)</td>
<td>0</td>
</tr>
<tr>
<td>Net Antennae (Tolerance=20mil) (All)</td>
<td>0</td>
</tr>
<tr>
<td>Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)</td>
<td>0</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>0</strong></td>
</tr>
</tbody>
</table>

### Rule Violations

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clearance Constraint (Gap=5mil) (All),(All)</td>
<td>0</td>
</tr>
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<td>0</td>
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<td>0</td>
</tr>
<tr>
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<td>0</td>
</tr>
<tr>
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<td>0</td>
</tr>
<tr>
<td>Power Plane Connect Rule(Relief Connect ) (Expansion=15.748mil) (Conductor Width=5.906mil) (Air Gap=5.906mil)</td>
<td>0</td>
</tr>
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<td>0</td>
</tr>
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<td>0</td>
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<td>0</td>
</tr>
<tr>
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<td>0</td>
</tr>
<tr>
<td>Silk To Solder Mask (Clearance=0mil) (IsPad),(All)</td>
<td>0</td>
</tr>
<tr>
<td>Silk to Silk (Clearance=0mil) (All),(All)</td>
<td>0</td>
</tr>
<tr>
<td>Net Antennae (Tolerance=20mil) (All)</td>
<td>0</td>
</tr>
<tr>
<td>Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)</td>
<td>0</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>0</strong></td>
</tr>
</tbody>
</table>
## Electrical Rules Check Report

<table>
<thead>
<tr>
<th>Class</th>
<th>Document</th>
<th>Message</th>
</tr>
</thead>
<tbody>
<tr>
<td>Warning</td>
<td>Project Page.SchDoc</td>
<td>Incorrect link between project variant &quot;Default Build&quot; and schematic component Component R3 1K5.0402 1%</td>
</tr>
<tr>
<td>Warning</td>
<td>Project Page.SchDoc</td>
<td>Incorrect link between project variant &quot;Default Build&quot; and schematic component Component R4 1K5.0402 1%</td>
</tr>
<tr>
<td>Warning</td>
<td>Project Page.SchDoc</td>
<td>Incorrect link between project variant &quot;Default Build&quot; and schematic component Component U1 TOF</td>
</tr>
<tr>
<td>Warning</td>
<td>Project Page.SchDoc</td>
<td>Incorrect link between project variant &quot;Default Build&quot; and schematic component Component U2 TOF</td>
</tr>
</tbody>
</table>
# Bill of Materials

**TMF8701 Daughter Card**

**Source Data From:** DC-TMF8701-01.PrjPcb  
**Project:** DC-TMF8701-01.PrjPcb  
**Variant:** None  
**Creation Date:** 20.03.2019 13:55:07  
**Print Date:** 20-Mar-19 1:55:18 PM

<table>
<thead>
<tr>
<th>Designator</th>
<th>Comment</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>Description</th>
<th>Alternate</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C2, C3</td>
<td>0.1uF,6V3, 0402, 10%, 0.1uF,6V3,0402, 10%</td>
<td>Murata Electronics North America</td>
<td>GRM155R70J104KA01D</td>
<td>Cap 0.1uF,6V3, 0402, 10%</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>C4</td>
<td>1.0uF,6V3, 0402, 20%</td>
<td>AVX</td>
<td>04026D105MAT2A</td>
<td>Cap 1.0uF,6V3, 0402, 20%</td>
<td>YES</td>
<td>1</td>
</tr>
<tr>
<td>CN1</td>
<td>CONN FFC TOP 14POS 0.50MM R/A</td>
<td>Molex</td>
<td>0545501471</td>
<td>CONN FFC TOP 14POS 0.50MM R/A</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>M1, M2, M3, M4</td>
<td>Mounting Hole</td>
<td>PennEngineering</td>
<td>SMTO-M1-1ET</td>
<td>Mounting nut 0.1&quot; Dia M1 thread</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>R1, R2, R5, R6</td>
<td>10K,0402,5%</td>
<td>Vishay Dale</td>
<td>CRCW040210K0JNEF</td>
<td>Res, 10K, 0402, 5%</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>U2</td>
<td>TOF</td>
<td>ams AG</td>
<td>TMF8701</td>
<td>TOF</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

**Approved Notes:**  
Parts with alternate marked as YES may be replaced by an equivalent with preapproval from AMS.  
Parts from ams AG will be consigned.