Product Document

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Application Note

TMD2772

I2C Timing Requirements

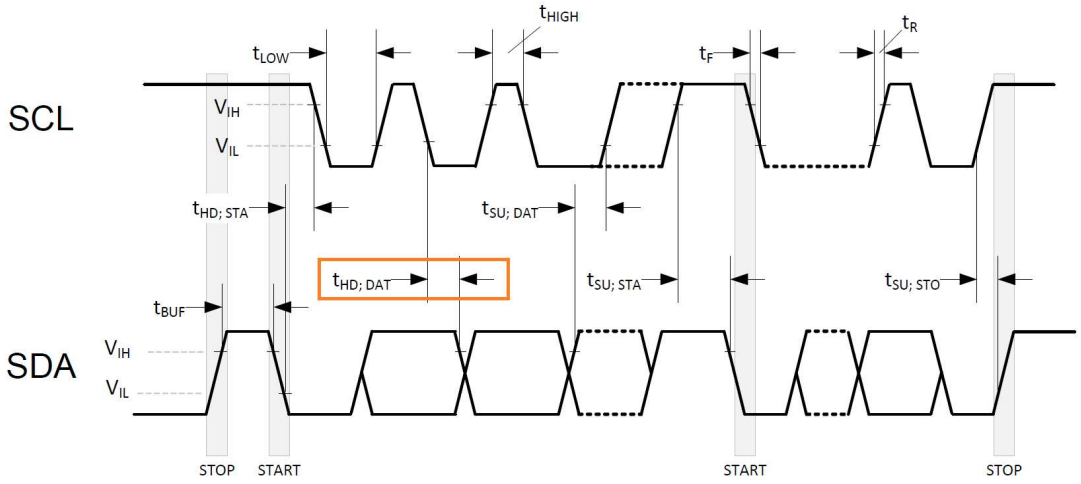
Content Guide

1 Overview

This application note applies for theTMD2772 device family comprising the TMD27721, TMD27723, TMD27725 and TMD27727.

2 General Description

ams had to change minimum data tHD;DAT (Data hold time) to 60ns. The data hold time is the time between the falling edge of SCL and the change of SDA – see below.



I2C specification (e.g. NXP Rev. 5 — 9 October 2012) specifies 0ns data hold time for slave in table 10 and allows for longer data hold times from the master according to footnote 4:

:

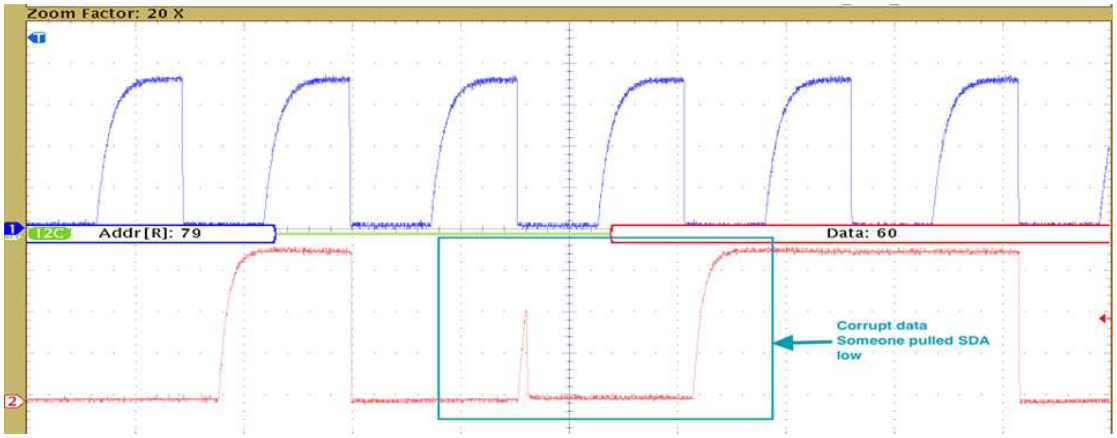
$t_{HD;DAT}$	data hold time[2]	CBUS compatible masters (see Remark in Section 4.1)	5.0	-	-	-	-	µs
		I²C-bus devices	0[3]	-[4]	0[3]	-[4]	0	- µs

[4] The **maximum tHD;DAT could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode**, but must be less than the maximum of tHD;DAT or tHD;ACK by a transition time. This maximum must only be met if the device does not stretch the LOW period (tLOW) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

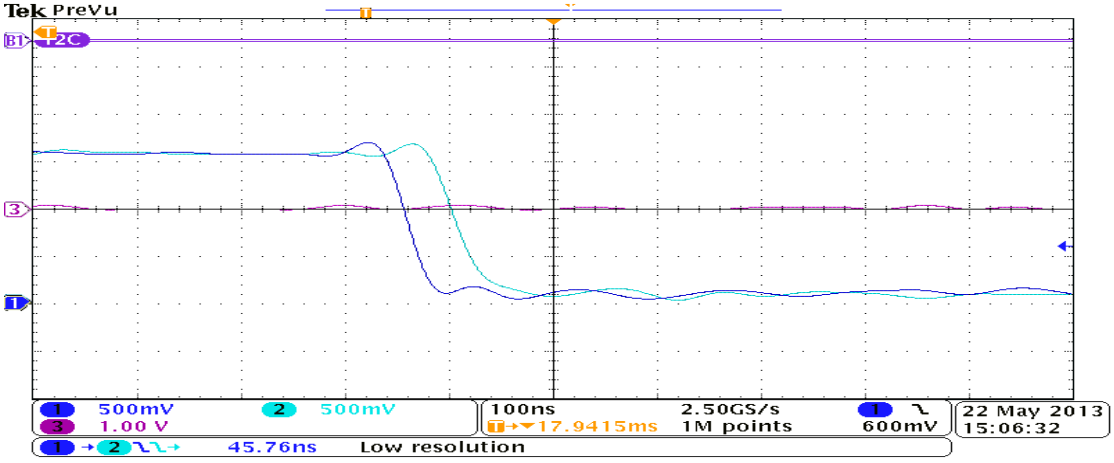
If the bus master uses less than 60ns tHD;DAT hold time, I2C communication could fail. This will affect both device read and device write, as a device read will always need a device write (I2C device address) just before.

3 Measurements of the tHD;DAT timings

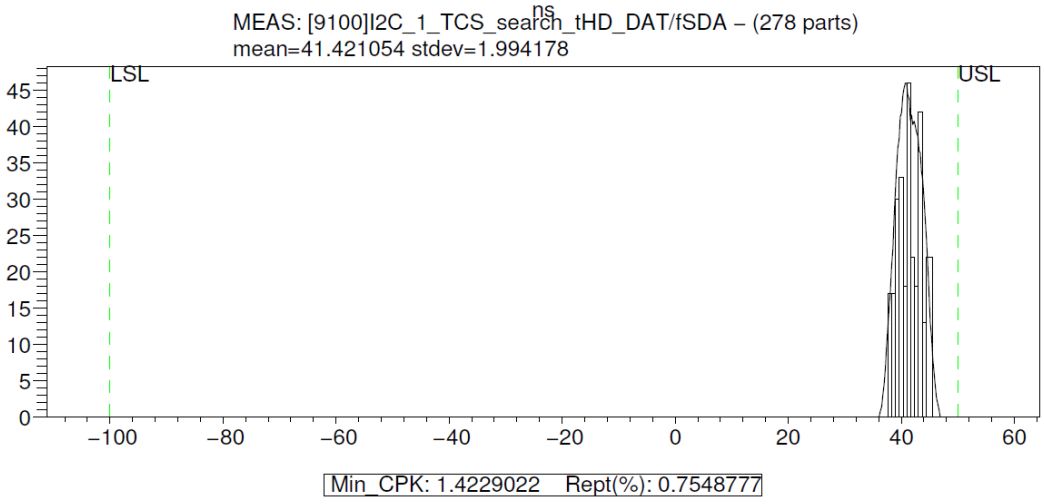
The following waveform is measuring a failed I2C communication:



Zoom in on the following edge: SCL falling edge only leads SDA by 20nS



Measuring the tHD;DAT over several parts (278) results in the following limits:



Additional simulations taking temperature and process into consideration show a required limit of tHD;DAT of 60ns.

Most bus masters do not use the minimum tHD;DAT specification of 0ns. There is a simple and compelling reason not to use 0ns timing: Slight differences between capacitive loads on SCL and SDA will move the timing slightly thus violating the I2C specification on the bus. Therefore most bus master usually use >0ns values for tHD;DAT.

4 Recommended operation

ams recommends to measure the tHD;DAT (falling edge of SCL to change of SDA) in the actual system. As bus master has the freedom to choose any time up to 0.9 µs (see above), however, the actual implementation operation can be ensured if the measured tHD;DAT is well above the 60ns.

5 Summary

Even if the 60ns tHD;DAT timing of TMD2772 is in contradiction to the I2C specification, most I2C masters usually do not go to the limits of the I2C specification. It is recommended to measure the actual timing the bus master uses and if it is well above 60ns, operation is guaranteed.

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8 Revision Information

Initial version 1-00

Changes from 1-00 (2014-Jun-26) to current revision 1-01 (2014-Sep-2014)	Page
Added section Overview	3

Note: Page numbers for the previous version may differ from page numbers in the current revision.