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INTELLIGENT OPTO SENSOR DESIGNER'S NOTEBOOK

Proximity Detection Layout Recommendations

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Overview

The TSL267x, TSL277x, and TCS377x devices are all capable of doing proximity detection. Internally the driver pulses an external IR LED with a selectable number of fast rise-time pulses which adds noise to the power distribution system. Selection of external passive components, supply regulators and attributes of the PCB layout will impact the performance of the device. This paper provides guidelines to reduce the noise generated and achieve consistent and reliable operation.

TAOS Proximity Architecture

The TAOS proximity systems require power to be connected to both VDD and LEDA connections in the figure below. The IR LED is momentarily pulsed by switching the LED cathode to ground (via the LDR pin) and controlling the sink current through it. Noise coupled onto VDD decreases the system performance and should be minimized.

The LDR pin is analogous to a constant-current sink but it varies with supply voltage and factory trim. With these variations it is best to budget a LDR sink current peak of 150mA through the IR LED. While Idd into the Vdd pin is typically less than 200uA when driving the LED it can peak as high as 3mA. The power supply (or supplies) must provide clean and stable power to these pins.



Figure 1. TAOS Proximity Sensor Architecture

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Power Source

TAOS proximity sensors amplify a very small current generated by internal optical photodiodes to quantify the amount of light present. The reflected IR signal (plus undesired background light) is measured then the background light is subtracted. The result is a very small amount of energy (representing the reflected signal) that is impacted by the noise on the power supply. This noise will cause variation in the offset of the proximity signal. By minimizing the noise with an optimized filter circuit and layout the offset of the device will be more stable and predictable.

Various types of power supplies are used including switching regulators and low dropout regulators (LDOs). In any case the LED pulses must be sourced and the fast rise times taken into account when designing the power regulator. Improperly designed circuits (especially LDO's) will oscillate and become unstable. Several aspects of the power supply design need to be considered:

- Selection of the power regulator type, number and maximum output current
- Large bulk capacitance for LED inrush current 10uF minimum (distributed or lumped)
- Regulator caps (switching or LDO) should be selected per manufacturers recommendations
- Low ESR output capacitors may cause oscillation See LDO recommendation
- Decoupling capacitors and PCB layout
- Trace widths and control of parasitics in the supply distribution system

Single vs Dual Supply

It is highly recommended that the LEDA and VDD supplies come from two separate sources as shown in Figure 2. Many systems already have a digital supply and a quiet analog supply. If using existing supplies connect the LED anode to the digital supply and VDD to the analog supply, making sure the digital supply has an adequate amount of power available to drive the LED (budget for 150mA).



Figure 2. Preferred application using two LDO regulators

In some cases, it is not feasible to provide two separate power supplies to the device. In this situation, the system design must be robust enough to ensure low noise drive to the proximity sensor. If the same supply is provided to both the LED anode and the Vdd pin, filtering must be used to reduce the noise present at the Vdd pin.

To improve supply isolation and provide ripple reduction an RC filter is used. When VDD >= 2.6V the series R = 22Ω and the shunt C = 1uF. If VDD < 2.6V the series R = 10Ω and the shunt C = 2.2uF. In each case the shunt capacitor is the one located closest to the device pin.

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Small physical component sizes can be used for the resistor since the current through it is very small. Figure 3 shows an approach using a single LDO regulator for both Vdd and the LED anode.



Figure 3. Application Using a Single LDO for Vdd and LED anode

A third option is to run the LED anode directly from the upstream regulator. This has the benefit of isolating the LED switching noise from VDD and also providing a regulated supply to the LED. The output voltage of the upstream regulator must be compatible with the maximum voltage specification for the LED in the TAOS datasheet.



Figure 4. Application Using a Single LDO with Switching Regulator sourcing LED anode

For portable applications it is possible to source the LED current directly from a battery but there are negative side effects. The battery voltage varies as it is charged causing potential device damage and also as it discharges creating variation in the current through the IR LED. In addition (and more significantly) load transients can create peak surge voltages that exceed the junction breakdown specification for the device. This can lead to catastrophic failures that are hard to analyze following device failure. The following may work but is not a preferred solution by TAOS:

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Layout Recommendations





Figure 5. Application Using a Single LDO & Battery sourcing LED anode

LDO Capacitors

LDO datasheets often recommend 2.2uF or 4.7uF output capacitors. This cap forms a pole in the transfer function on devices with PNP or PMOS pass elements and impacts output stability. For systems with a separate Vdd supply regulator this recommendation will work well.

For the LED anode careful analysis of the transfer function is the only way to guarantee stability. Larger distributed capacitance (10uF min, 22uF recommended) has proven to be a good general recommendation. Using a 4.7uF capacitor placed close to the LDO and 4.7uF or 10uF closer to the LED is a good low cost solution. If a flex assembly is used (containing the sensor and LED) the second 4.7uF cap can be mounted on the motherboard close to the flex assembly connector. Low ESR electrolytic caps are not recommended.

PCB Layout

Figure 6 shows a layout for a device with an OSRAM SFH4650 IR LED which is used on the TAOS EVM daughter-boards. The layout minimizes the footprint of the sensor while keeping the component close to the device and keeping the overall footprint small. C1 is the 1uF bypass for the sensor. R8 is the series resistor and C3 is the 1uF bypass capacitor adjacent to the LED. The 22uF capacitor is on the motherboard close to the LDO which provides the regulated 3V supply voltage. The components are 0402 (1005 metric) size.



Figure 6. Single LDO recommended passive placement (shown on double sided PCB)

Power traces should be kept on the same side of the PCB or flex circuit as the sensor and LED minimizing the number of vias. Minimum trace widths of 20 mils are recommended for LEDA and the ground return path. With power planes the ground return path should be unbroken between the sensor and the supply.

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