NSE5310 – OTP – Programming Application Note

NSE5310

OTP Programming Application Note

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Revision History

Revision	Date	Owner	Description
1.0	August, 26.2011		• Added OTP Assignement table
0.01	August, 26.2011		• First draft
1.01	July, 2.2013	azen	• Edited with new ams Template

1 General Description

This application note describes the programming of the one-time programmable bits of the NSE-5310. Following, permanent programming, writing and reading of the OTP Latch as well as techniques for verification after programming are shown.

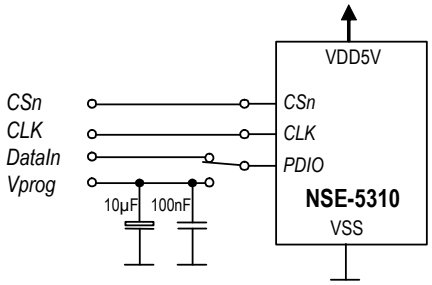
For an overall product description refer to the NSE-5310 datasheet.

2 OTP Memory Programming

2.1 Hardware Connections

To access the OTP memory, you need the three signals PDIO, CSn and CLK. The NSE-5310 can be programmed in 3.3V or 5V mode. The related programming voltage is always between 3.3V and 3.8V.

Figure 1 Programming circuit of NSE-5310

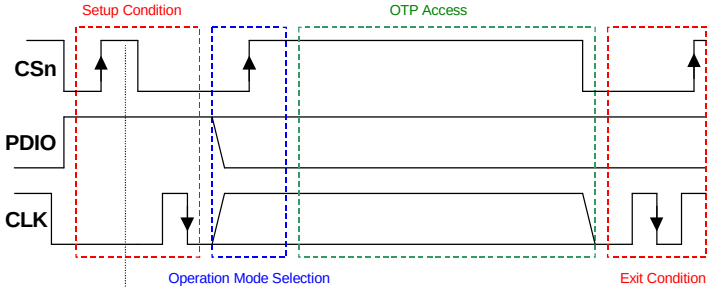


2.2 One Time Programmable Register (OTP)

The OTP Register should add flexibility to the user. It allows activating of different features of the NSE-5310 miniature position encoder.

By default the periphery pins CSn, CLK and PDIO are used for the interface and daisy chain configuration. To access the OTP register, a special setup condition must be performed. Another exit condition must be performed to get out of the access mode.

Figure 2 OTP register input and exit condition



2.3 OTP Bit Assignment

The table below shows the different OTP bits available for the NSE-5310.

Bit	Symbol	Function	Typ	Note
	Mbit1	Factory Bit 1		
51	PWMhalfEN_IndexWidth	V_{PDIO}=100mV	Customer Section	
50	MagCompEN			
49	pwmDIS	Disable PWM		
48	Output Md0	Default; 10 bit inc.; 12 bit inc; Sync mode;		
47	Output Md1			
46:35	Z<0:11>	Zero position		
34	CCW	change inreasing / decreasing code with encoder movement		
33:29	I2C_A <1:5>	I2C Address		
28:0	Factory Section			
	Mbit2	Factory Bit 0		

Table 1 OTP Bit Assignment

2.4 AUTOLOAD Operation

The AUTOLOAD Operation is performed at every power on sequence and transfers permanent stored data from each PolyFuse to its corresponding latch. The outputs of the registers are internally available and buffered in parallel format.

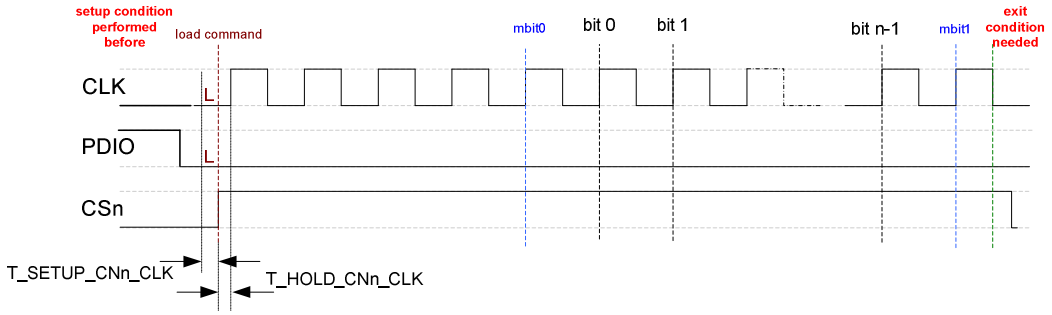
2.5 LOAD Operation

The LOAD Operation transfers permanent stored data from each PolyFuse to its corresponding latch on demand.

At CLK=LOW and PDIO=LOW the rising edge on CSn signal latches the load command internally. Each rising edge at CLK gets another bit stored into the register. There are n+7 rising edges necessary to load all data. The next falling edge will stop the load operation.

This mode is not recommended in application because the asynchronously change (bit after bit). A power down and AUTOLOAD can be used instead.

Figure 3 PPTRIM LOAD operation



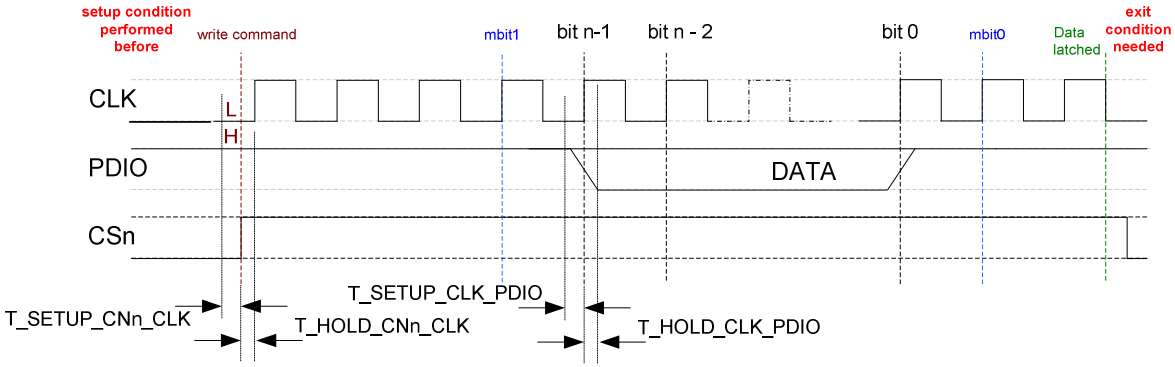
2.6 WRITE Operation

The WRITE Operation writes DATA from the PDIO pin into the internal latch. The operation stops automatically after DATA is latched.

This operation is started by CLK=LOW and PDIO=HIGH during rising edge of CSn signal. All external data will be shifted into an internal latch chain.

DATA must be stable at rising edge of the CLK signal.

Figure 4 PPTRIM WRITE operation

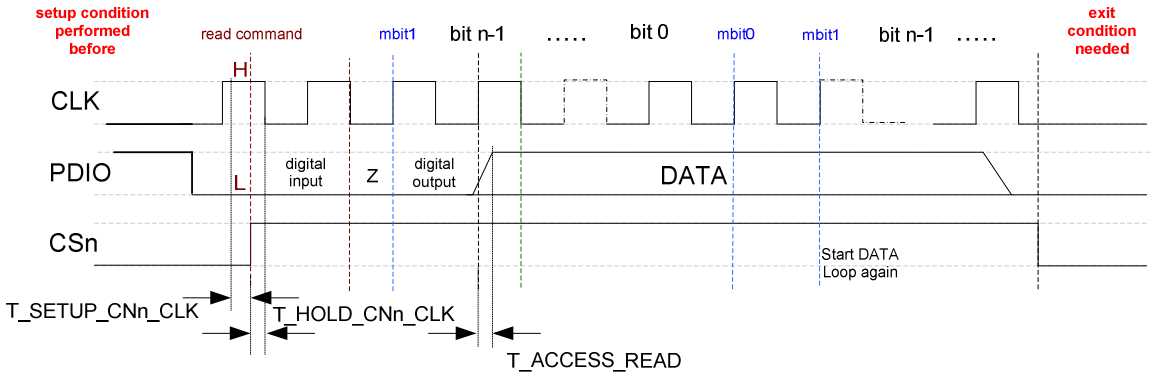


2.7 READ Operation

The READ Operations transfers DATA from internal latches to the PDIO pin. DATA is looping until CSn=LOW stops the operation.

This serial read of the register data is started with CLK=HIGH and PDIO=LOW during rising edge of the CSn signal. The signal PDIO works in data out direction after the second rising edge at CLK.

Figure 5 PPTRIM READ operation

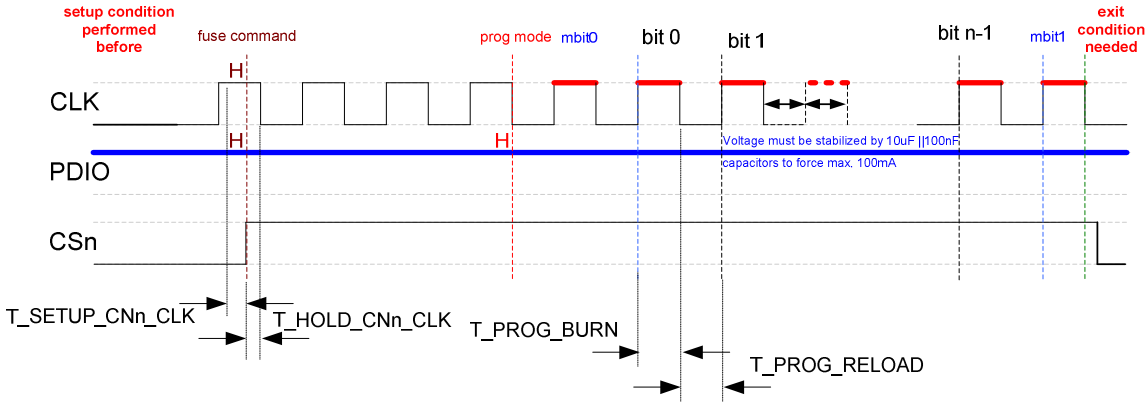


2.8 PROG Operation

The PROG Operation burns DATA that was written to the latch before, permanent into polyfuses.

PDIO=HIGH and CLK=HIGH during rising edge of CSn signal starts this operation. The fusing is managed bit by bit due to the high current need for fusing. The programming time of PolyFuse cell is defined by the high pulse of CLK (PROG_BURN). As there is a maximum current of 100mA needed for permanently fusing, PDIO has to be stabilized by some capacitance during this operation. The low time of CLK (PROG_RELOAD) allows to recharge the capacitor. This is useful if the source has a limited current and can be compensated by increasing this time.

Figure 6 PPTRIM PROG operation



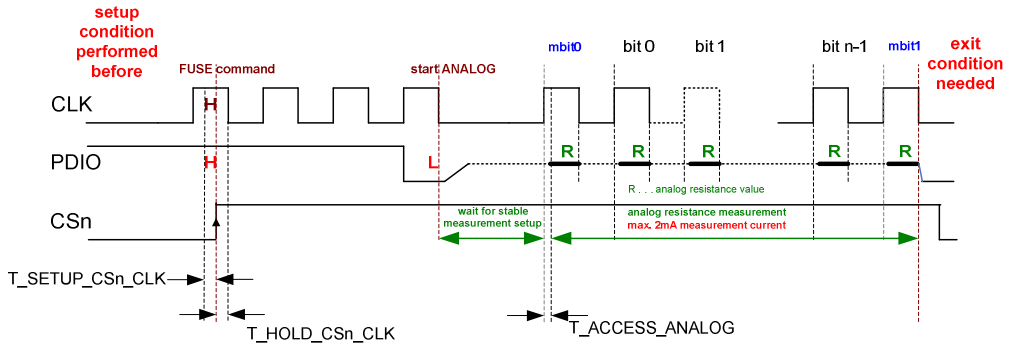
2.9 ANALOG Operation

The ANALOG Operation allows reading the resistance of a polyfuse.

Setting a maximum voltage of 100mV on PDIO before second falling edge of CLK during PROG operation allows measuring the current through a PolyFuse.

Non programmed PolyFuses have a resistor of about 50-100Ohms (1-2mA), programmed PolyFuses have a typical resistor higher than 100kOhms up to infinite resistance (0-2µA). The comparator level is in a range of 1kOhm.

Figure 7 PPTRIM ANALOG operation



This operation is defined in a similar way than the PROG operation. At the 4th falling edge of PCLK, PDIO must be LOW, further on internal switches enable the analogue resistance measurement between PDIO pad and GND. Two rising edges of PCLK later, the first polyfuse resistance (mbit0) can be measured during PCLK= HIGH. At each following PCLK=HIGH, one polyfuse after the other is measured.

During resistance measurement, the maximum current must not exceed 2mA, to avoid unwanted programming to the PolyFuse elements.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{unprog}	Current for unprogrammed Polyfuse	V_{PDIO}=100mV	0.5	1.4	2	mA
I_{prog}	Current for programmed Polyfuse	V_{PDIO}=100mV	-	0.1	10	µA

3 Operating Conditions

3.1 Operating Conditions for PROG Operation

Parameter	Symbol	Min	Max	Unit	NOTE
Positive Supply Voltage (1) (=Programming Voltage)	VDD	3.3 3.5	3.6 3.6	V V	Positive supply for Temp < 70°C Positive supply for Temp < 150°C
Negative Supply Voltage	VSS	0	0	V	Ground =0V
Junction Temperature	$T_{junction}$	0	150	°C	High temperature can cause a higher programming yield loss !
Programming Current into PDIO	$I_{PDIO,prog}$		100	mA	required current to program a single PolyFuse element (2)
Programming refresh time	$t_{PROG\_REFRESH}$	1.0		µs	minimal refresh time during fusing – pad CLK (3)
The PolyFuse can be programmed only once					

Notes:

(1) The supply voltage must be fixed in the same range than the programming voltage

(2) The PolyFuse cells are programmed in a bit by bit sequence due to the high current at fusing.

Refreshing time of the external capacitor depends on the compliance current of the fusing voltage source.

3.2 AC Characteristics: Timing Specifications

Parameter	Description	Min	Typ	Max	UNIT
$T_{\_SETUP\_CSn\_CLK}$	Setup time for operation	5			ns
$T_{\_HOLD\_CSn\_CLK}$	Hold time for operation	10			ns
$T_{\_SETUP\_CLK\_PDIO}$	Setup time for data	5			ns
$T_{\_HOLD\_CLK\_PDIO}$	Hold time for data	10			ns
$T_{\_ACCESS\_READ}$	Access time for data			60	ns
$T_{\_PROG\_BURN}$	Programming time	10	15	20	µs
$T_{\_PROG\_RELOAD}$	Reload time of programming cap.	10			µs
$T_{\_ACCESS\_ANALOG}$	Delay time of analog read of PolyFuse			10	µs

3.3 Operating Conditions for ANALOG Operation

Parameter	Symbol	Min	Max	UNIT	NOTE
Analog Voltage	V_{analog}	90	100	mV	Set on PDIO(1)
Analog Current Prog. Fuse	$I_{ana,1}$	0	10	uA	10kOhms - infinite(1)
Analog Current Unprog. Fuse	$I_{ana,0}$	1	2	mA	50 - 100 Ohms (1)
Setup time for operation mode	$T\_{Setup\_MODE\_PCLK}$	5		ns	
Hold time for operation mode	$T\_{HOLD\_MODE\_PCLK}$	10		ns	
Polyfuse					

Notes: (1) The resistor or the PolyFuse can be calculated by setting a maximal voltage of 100mV on PDIO during PROG operation and measuring the current into the pin.

4 Test Sequence

4.1 Check AUTOLOAD

1) AUTOLOAD operation triggered with Power Up
2) READ operation: Data must be 0 for all bits (for non programmed devices)

4.2 Check Serial Interface

3) WRITE operation of checkerboard pattern (1010..)
4) READ operation data has to read checkerboard pattern
5) WRITE operation of anti checkerboard pattern (0101..)
6) READ operation data has to read anti checkerboard pattern

4.3 Check Comparator

7) WRITE operation: Every bit high (1111..)
8) LOAD operation performed to non programmed PolyFuses
9) READ operation: Data must be 0 for all bits (for non programmed devices)

4.4 Get Trimming Pattern

10) Test of user specific non trimmed parameter.
11) WRITE operation to trim parameter.

4.5 Program PolyFuses

12) PROG operation performed to program trimming pattern into PolyFuses.

4.6 Check programmed Pattern

13) AUTOLOAD operation (LOAD operation if AUTOLOAD will be performed on later tests)
14) READ operation: Compare digital pattern with trimming pattern
15) ANALOG operation: Read analog resistance levels for PolyFuses
16) Calculate maximum resistance value for non programmed PolyFuses
17) Calculate minimum resistance value for programmed PolyFuses
18) Retest of user specific trimmed parameter.

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