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Application note for CMV sensors

Design and Layout Practices

Change record

Issue	Date	Modification
v1	15/7/2015	Origination, based on CMV2000 AN07

Table of Contents

1 INTRODUCTION

This document describes design and layout guidelines, mostly regarding the high speed LVDS signals, to keep in mind when designing a PCB or camera system for CMV series sensors.

For a more detailed look on high speed LVDS layout and design, please refer to *The LVDS Owner's Manual, 3rd Edition, Spring 2004* of National Semiconductors.

2 SENSOR INTERFACE

The CMV sensors have basically two kinds of signal I/O types:

- High Speed digital I/O (LVDS_OUT's, LVDS_CLK_IN input)
- 'Slow' CMOS/TTL digital I/O (SPI, CLK_IN, FRAME_REQ, T_EXP1/2,SYS_RES_N)

The LVDS I/O's are in compliance with the EIA/TIA-644A standard. Actual voltage levels can differ from the specification, always refer to the sensor datasheet for the exact voltage levels. Traces carrying these high speed signals should be treated as transmission lines. The fast edge rate of an LVDS driver means that impedance matching is very important – even for short runs. Matching the differential impedance is important. Discontinuities in differential impedance will create reflections, which will degrade the signal and also show up as common-mode noise. Common-mode noise on the line will not benefit from the canceling magnetic field effect of differential lines and will be radiated as EMI.

Controlled differential impedance traces should be used as soon as possible after the signal leaves the IC. Try to keep stubs and uncontrolled impedance runs to <12 mm or 0.5 in. Also, avoid 90° turns since this causes impedance discontinuities; use 45° turns, radius or bevel PCB traces.

Minimize skew between conductors within a differential pair. Having one signal of the pair arrive before the other creates a phase difference between voltages along the signal pairs that appear and radiate as common-mode noise.

Use bypass capacitors at each package and make sure each power or ground trace is wide and short (do not use 50Ω dimensions) with multiple vias to minimize inductance to the power planes.

3 PCB DESIGN AND LAYOUT

3.1 PCB DESIGN

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals. Dedicating planes for V_{CC} and ground are typically required for high-speed design. The solid ground plane is required to establish a controlled (known) impedance for the transmission line interconnects. A narrow spacing between power and ground will also create an excellent high frequency bypass capacitance.

Isolate fast edge rate CMOS/TTL signals from LVDS signals; otherwise the noisy single-ended CMOS/TTL signals may couple crosstalk onto the LVDS lines. It is best to put TTL and LVDS signals on (a) different layer(s), which should be isolated by the power and ground planes.

Keep drivers and receivers as close to the sensor connections as possible. This helps to ensure that noise from the board is not picked up onto the differential lines and will not escape the board as EMI, from the (cable) interconnect. This recommendation also helps to minimize skew between the lines. Skew tends to be proportional to length; therefore, by limiting length, we also limit skew.

Pin dimensions vary per sensor model. In general, when soldering the sensor directly on the PCB, the maximum board thickness is limited to ensure good solder joints with the pins. For example, for a 2.7mm pin, the thickness is limited to 2.30mm.

When possible, use sockets for the image sensors so that they are removable from the board without desoldering. In case of an RMA, this makes it much easier to test sensors and replace them. CMOSIS cannot desolder sensors from PCBs, this will have to be done at the customer's side. Another reason to use a socket is that desoldering can also cause further damage the sensor, and make interfacing difficult due to solder residue on the sensor pins.

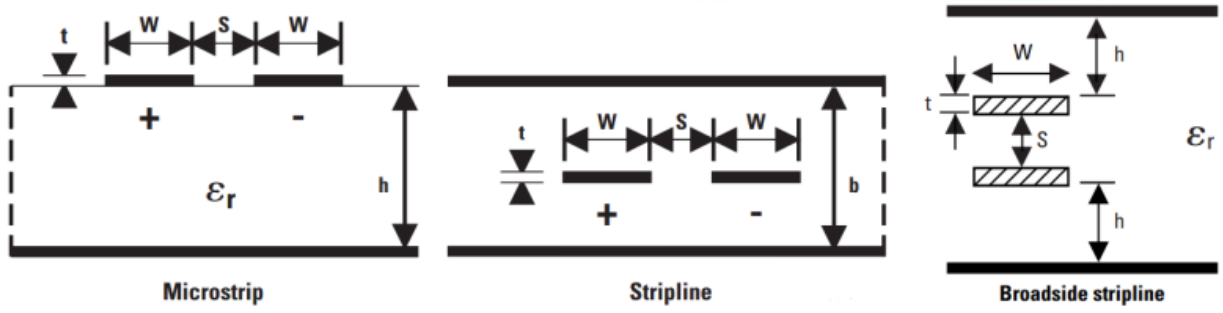
3.2 LVDS TRACES LAYOUT

Edge-coupled microstrip, edge-coupled stripline, or broad-side striplines all work well for differential lines.

Traces for LVDS signals should be closely coupled and designed for 100Ω differential impedance.

Edge-coupled microstrip lines offer the advantage that a higher differential Z_O is possible (100Ω to 150Ω). Also, it may be possible to route from a connector pad to the device pad without any via. This provides a "cleaner" interconnect. A limitation of microstrip lines is that these can only be routed on the two outside layers of the PCB, thus routing channel density is limited.

Stripline may be either edge-coupled or broad-side coupled lines. Since they are embedded in the board stack and typically sandwiched between ground planes, they provide additional shielding. This limits radiation and also limits coupling of noise onto the lines. However, they do require the use of vias to connect to them.



Use controlled impedance PCB traces that match the differential impedance of your transmission medium (e.g., cable) and termination resistor. Route the differential pair traces as close together as possible (use the minimum spacing "S" specified by your PCB vendor) and as soon as they leave the sensor. This helps to eliminate reflections and ensures that noise is coupled as common-mode.

The value of dielectric constant (ε_r) varies for different PCB materials. This constant will influence your impedance. Also note that ε_r will vary within a single board. It is not uncommon for FR-4 PCBs to vary by 10% across one board, affecting skew. This is another good reason to keep differential lines close together.

Match electrical lengths between traces of a pair to minimize skew. Skew between the signals of a pair will result in a phase difference between the signals. That phase difference will destroy the magnetic field cancellation benefits of differential signals and EMI will result! A general rule is to match lengths of the pair to within 100 mils.

Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match trace length and to ensure isolation between pairs of differential lines.

Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels instead.

Within a pair of traces, the distance between the two traces (S) should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable. The key to “imbalances” is to make as few as possible and as small as possible. Differential transmission works best on a balanced interconnect. For the best results, both lines of the pair should be as identical as possible.

3.3 LVDS TERMINATION

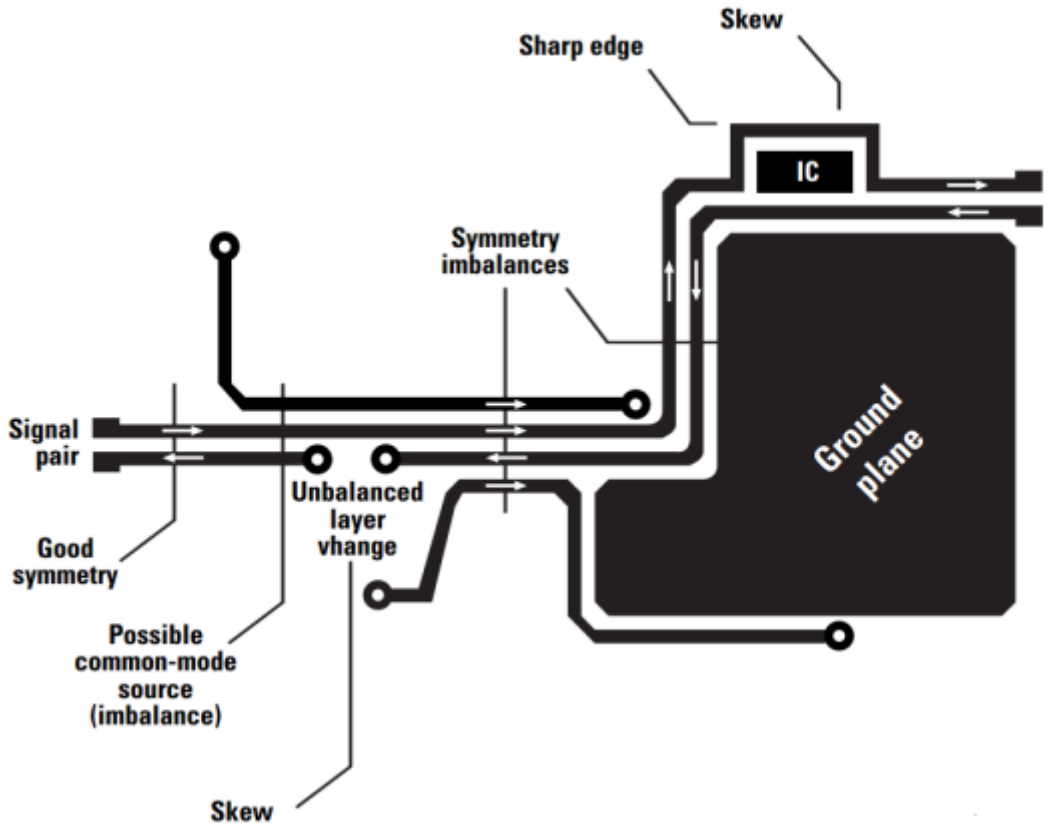
Use a termination resistor that best matches the differential impedance of your transmission line. It should be between 90Ω and 130Ω for point-to-point cable applications. Remember that the current-mode outputs need the termination resistor to generate the proper differential voltage. LVDS is not intended to work without a termination resistor. Typically, a single, passive resistor across the pair at the receiver end suffices. You could also use the internal termination in the FPGA if available.

Surface mount resistors are best. PCB stubs, component leads, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be <7 mm (12 mm max.).

Resistor tolerance of 1% or 2% is recommended. Note that from a reflection point of view, a 10% mismatch in impedance causes a 5% reflection. The closer the match, the better. Match it to the nominal differential impedance of the interconnect.

The distance between two pairs should be >2S. The distance between a pair and a TTL/CMOS signal should be >3S at a minimum. Even better, locate the TTL/CMOS signals on a different plane isolated by a ground plane. If a guard ground trace or ground fill is used, it should be >2S away.

On the picture below you can see many sources of differential signal imbalance that will influence signal integrity.



A conductor that carries current requires an opposite mirror current to return through some part of the system. This return current path will be the path of least resistance. For high-speed signals, the return current path will be the path of least inductance.

Since LVDS is differential, the signal current that flows in one conductor of a pair will flow back through the other conductor, completing the current-loop. This is ideal, because the current return antenna loop area is minimized since the traces of a pair are closely spaced. Real signals, however, will have some common-mode noise current, which must return also. This common-mode current will be capacitively coupled to ground and return to the driver through the path of least inductance. Therefore, a short ground current return path is needed between the driver and receiver in differential systems.

On PCB's, the best current return path is a uniform, unbroken ground plane beneath the LVDS signals. The ground plane will allow the common-mode (even mode) current to return directly under the LVDS signals. This closely coupled path is the path of least inductance and means that the current loop area is minimized.

Similarly, in cables, a ground return wire or wires should be used between driver and receiver. This allows the return path to be in close proximity to the signal pairs reducing the current loop area.

Shielding is an effective way to reduce EMI. Shielding should be connected directly to both driver enclosure and receiver enclosure when possible. Shields are not designed to handle significant ground return currents, so it may be necessary to construct a filter network which isolates the shield from ground at one end.

4 POWER SUPPLIES

Connect all ground and power pins directly to their respective ground or power plane. First tying them together and then connecting them to the respective plane tends to increase inductance and ground/power bounce and should be avoided.

Please use linear power regulators when possible. Switching power supplies can induce noise and ripple to the sensor and traces.

Place large decoupling capacitors directly at the output of the voltage regulator to filter low noise and improve peak current supply. Refer to the sensor datasheets for exact recommendations. We always advise to strictly follow these recommendations, because image sensors can have very big variations in power consumption, with significant peaks and troughs when the image sensor is grabbing images.