Product Document

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Application Note

AS726xN

Design Considerations

Content Guide

1 General Description

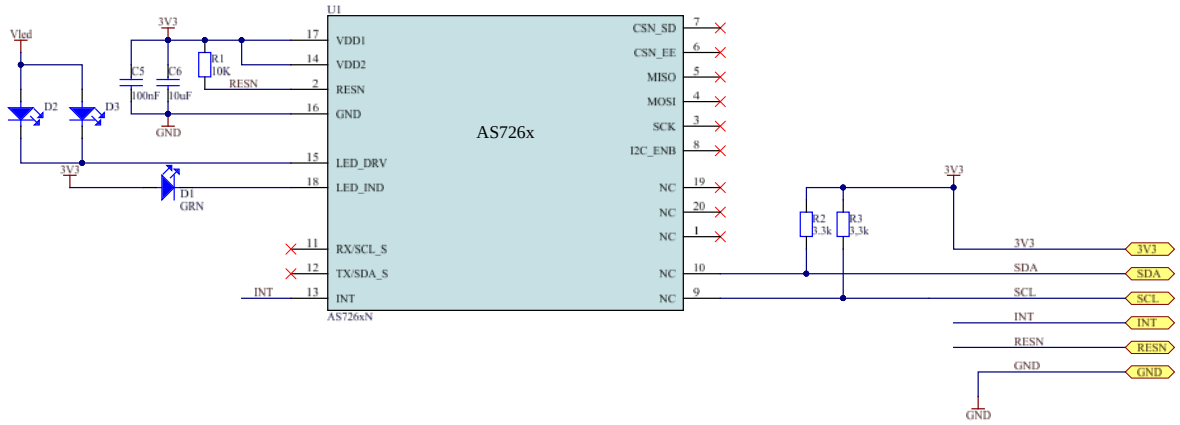
This Application Note briefly describes AS726xN system level design considerations.

2 Hardware Design Considerations

2.1 Typical Schematic

The typical schematic in Figure 1 shows AS726xN connection.

Figure 1. Typical Schematic



2.2 I²C Interface

The AS726xN sensor provides an I²C slave interface with the pin9, SCL, assigned to the bus clock and the pin10, SDA, for the bus data.

According to I²C specification, both SCL and SDA are open drain and need to be connected to a positive supply voltage via a pull-up resistor. The pull-up resistors, R2/R3 in the typical schematic, pull the line high when it is not driven low by the open drain interface. The maximum value of the pull-up resistor is limited by the bus capacitance, C_b, and the rise time, t_r, as below.

$$R_{P(max)} = \frac{t_r}{(0.8473 * C_b)}$$

The bus capacitance is the total capacitance of wire, connections, and pins. I²C Bus specifies the maximum rise time is 300ns.

On the other hand, the minimum value of the pull-up resistor depends on the device logical specifications and allows V_{OL} level to be read as a valide logical low.

$$R_{P(min)} = \frac{V_{DD} - V_{OL(max)}}{I_{OL}}$$

For the AS726xN application with 3.3V supply voltage, 0.4V maximum V_{OL}, and the specified minimum sink current of 3mA for standard mode (100KHz) or fast mode (400KHz), the minimum pull-up resistor value is 966.7Ω.

Then the decision of the pull-up resistor value would be based on the rise time, the total bus capacitance, and the power budget. A smaller resistor may get short rise time but has higher power consumption.

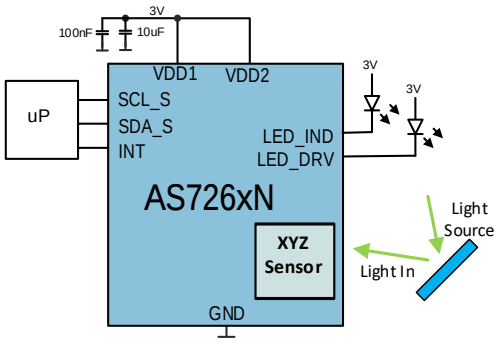
2.3 Power Connection

The AS726xN device requires a 2.7V - 3.6V supply on both VDD1 and VDD2 pins associated with the decoupling capacitors, C5/C6 in the schematic.

2.4 Light Source

2.4.1 Light Source Selection

Figure 2. Typical Application



A typical AS726xN application is to shine light rays to a target and AS726xN produces outputs based on the reflected light rays as Figure 2. So light source selection is determined by the spectral responsivity of reflected light and characteristics of the target. For example, if the target is expected to absorb 680nm light and the application needs to distinguish the target from others, a broadband white LED might be used as the light source with AS726xN, which has 680nm channel. Various applications may require different light sources.

2.4.2 Light Source Control

AS726xN implements two LED drivers. One has the programmable output of 1mA, 2mA, 4mA, or 8mA, which can be used for indication LED, D1 in the typical schematic. The other one can drive LEDs with the output current 12.5mA, 25mA, 50mA, or 100mA.

AS726x can also work with external LEDs.

3 PCB Layout Considerations

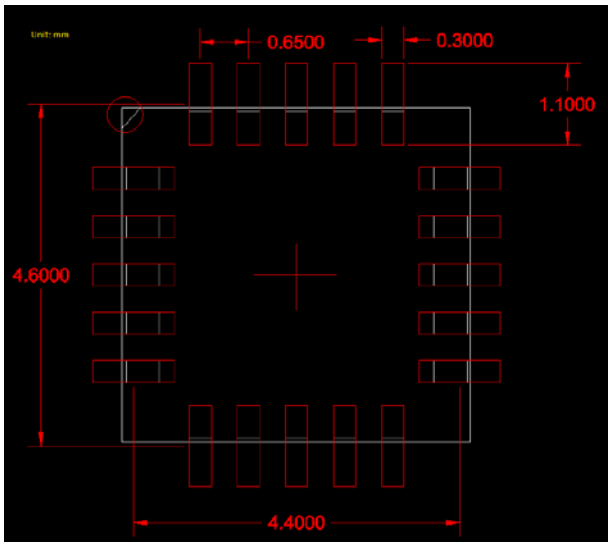
The generic PCB layout rules for digital designs should apply. In general, the wiring must be chosen so that crosstalk and interference to/from the bus lines is minimized. The I^2C bus specification also recommends that place VDD and/or GND between SDL and SDA if the traces are longer than 10cm.

The length of I^2C bus depends on the load of the bus and the speed you run at. The I^2C bus specification defines the maximum capacitance of the bus is 400pF. This bus capacitance limit is specified to limit rise time reductions and allow operating at the rated frequency. In general, with lower frequency and/or lower capacitance of the bus, you can have longer bus length.

For most of I^2C bus designs, the capacitance limit should be not the problem at all. If you design involves some unusual conditions, the specification has several strategies to cope with excess bus capacitance. For example, higher drive outputs, bus buffers, switched pull-up circuit etc. Please refer to the specification Section 7.2.

3.1 Footprint

Figure 3. AS726xN PCB Footprint Recommendation

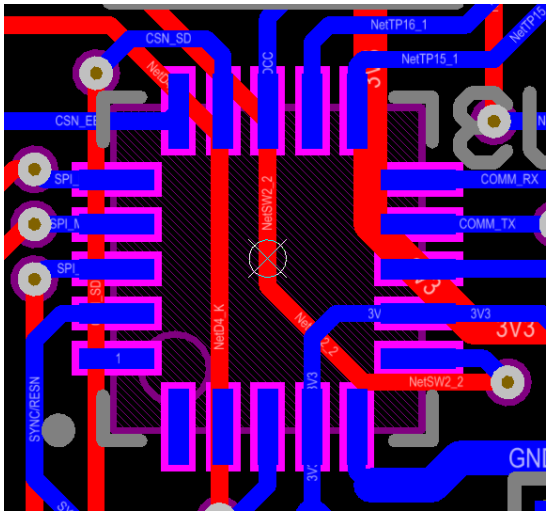


ams provide the schematic symbol and PCB layout footprint in Altium Design format. Please contact ams support team to get the library file.

3.2 Layout Recommendations

The recommendations to the layout are to place the decoupling capacitors C5/C6 closed to VDD pins of AS726xN device and to avoid to put any via underneath the device. Please refer to the Figure 4.

Figure 4. Sample Layout of AS726xN Device



3.3 LGA Population Recommendation

Please install the device align with the pads well. Also please make sure all pins would be firmly soldered on the pads.

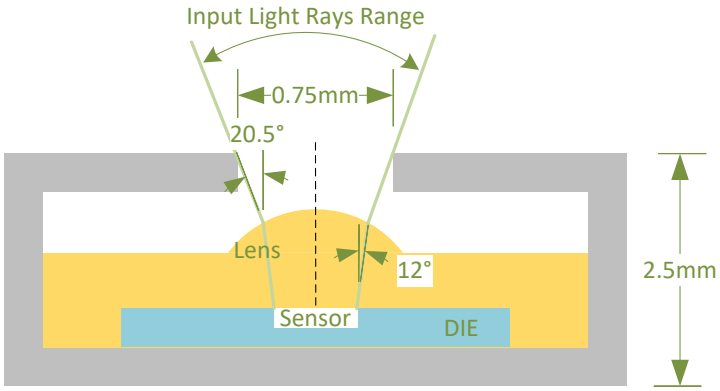
3.4 Optic Considerations

AS726xN has an open aperture on the surface. The diameter is 0.75mm and the package field of view is ±20.5°. In order to get accurate sensor data, the angle of the incident light should be carefully designed so that enough light would fell into the range of field of view. On the other hand, the amount of light should be controlled well to avoid the sensor situation.

Since there are six photo diodes in each AS726xN device, the incident light rays on each photo diodes should be even. For most reflection applications, the target may diffuse light well enough. If not, extra diffuser may be used between the target and AS726xN device.

As an open-aperture device, precautions must be taken to avoid particulate or solvent contamination as a result of any manufacturing processes, including pick and place, reflow, cleaning, integration assembly and/or testing.

Figure 5. Aperture with FOV



4 Software Design Consideration

In most of system designs, AS726xN is controlled by a microcontroller. The microcontroller software design should satisfy both I2C specification and AS726xN register programming sequence.

4.1 I²C Features

AS726xN supports both standard mode and fast mode. The 7-bit slave address is 0x49 and the addressing mode is 7+1-bit so when the controller send a read command to AS726xN, the slave address and R/W bit should be 0x93 and when sending the write command, it should be 0x92. Both read and write are single byte process. AS726xN does not support the slave clock stretching mode.

4.2 I²C Register Read/Write Commands

To read a register data from AS726xN, the read command should look like Figure 6.

Figure 6. I²C Register Read Command

Start	0x92	Reg Addr	Ack	Repeat Start	0x93	Reg Data	Nack	Stop

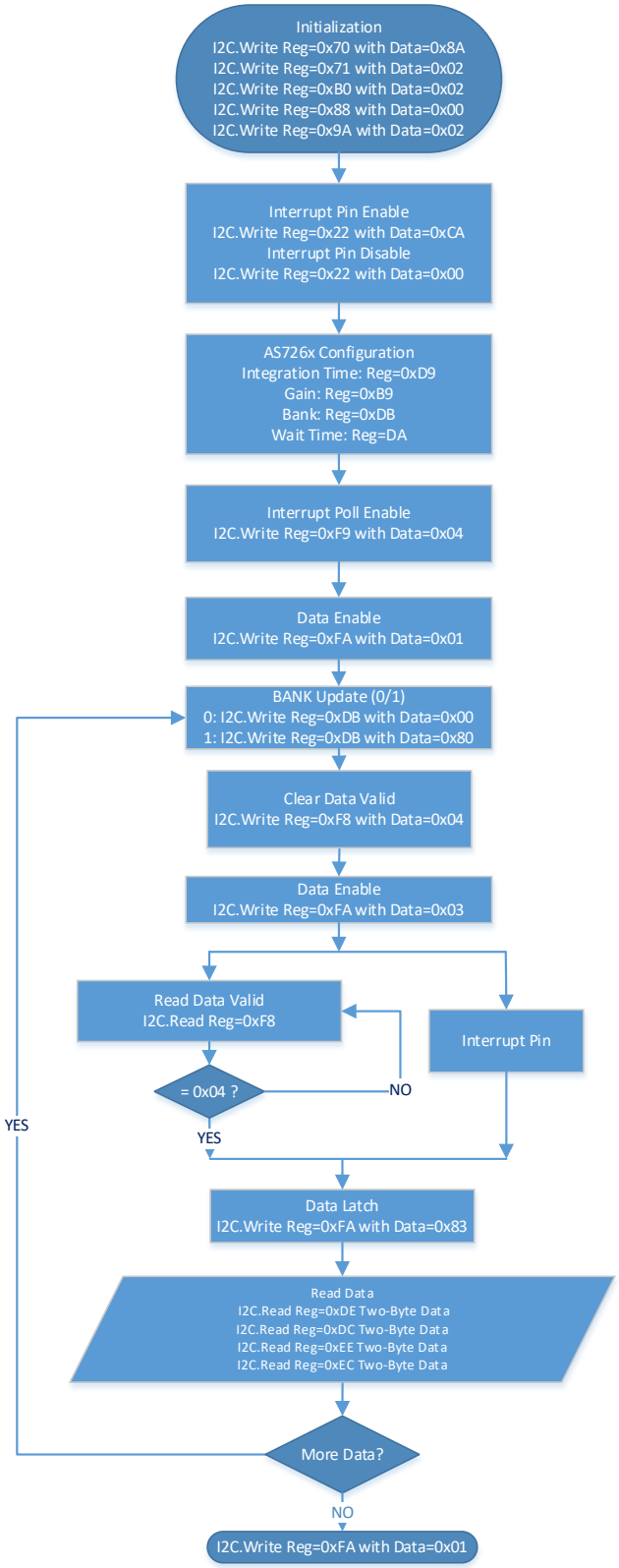
To write a value to a register of AS726xN, the write command should look like Figure 7.

Figure 7. I²C Register Write Command

Start	0x92	Reg Addr	Ack	Reg Value	Ack	Stop

4.3 Programming Sequence

Figure 8. Flow Chart



4.3.1 AS726xN Initialization

AS726xN require the initialization sequence to start a work. After power up or reset, issue the following I^2C register write commands in the order to AS726xN device.

Write register 0x70 to 0x8A

Write register 0x71 to 0x02

Write register 0xB0 to 0x02

Write register 0x88 to 0x00

Write register 0x9A to 0x02

4.3.2 Interrupt Pin Enable

Pin 13 can be enabled as the interrupt pin by writing register 0x22 to 0xCA. If interrupt is not needed, it can be disabled by writing register 0x22 to 0x00.

4.3.3 AS726xN Configuration

Select sensor Bank by programming register 0xDB, bit7. Write register 0xDB to 0x80 for Bank Mode 0 and write register 0xDC to 0x00 for Bank Mode 1.

Addr: 0xDB		BANK		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	BANK	0	R/W	0: Bank Mode 0; 1: Bank Mode 1
6:0	RSVD	0	R/W	Reserved, set to ‘b0000000 if writing the register

Set the Integration Time by programming register 0xD9. For example, write register 0xD9 to 0xC5 to configure the integration time to ~165.2ms.

Addr: 0xD9		INT_T		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	INT_T	0xFF	R/W	Integration time = <256 - value> * 2.8ms

Program Gain and LED_DRV current with the register 0xB9 if AS726xN is used to drive the light source.

Addr: 0xB9		GAIN_IDRV		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	IDRV	0	R/W	‘b00:100mA; ‘b01:50mA; ‘b10:25mA; ‘b11:12.5mA
5:2	RSVD	0	R/W	Reserved, set to ‘b0000 if writing the register
1:0	GAIN	0	R/W	‘b00: 1x; ‘b01: 3.7x; ‘b10: 16x; ‘b11: 64x

Program the Wait Time by writing register 0xDA.

Addr: 0xDA		INT_WT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	INT_WT	0xFF	R/W	Integration wait time = <256 - value> * 2.8ms

4.3.4 Interrupt Polling Enable

Program register 0xF9, bit2 to enable channel data ready by writing 0x04 to register 0xF9.

Addr: 0xF9		INT_POLL_EN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	RSVD	0	R/W	Reserved, set to ‘b00000 if writing the register
2	EN	0	R/W	1: Enable the channel data ready for polling or interrupt
1:0	RSVD	0	R/W	Reserved, set to ‘b00 if writing the register

4.3.5 Data Enable, Data Ready, and Data Latch

The sensor data can be read via the loop of Data Enable, Data Ready (Interrupt or Polling), and Data Latch.

Addr: 0xFA		DATA_EN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	DL	0	R/W	Data Latch. Set to 1 to latch the data after acquisition completes
6:4	RSVD	0	R/W	Reserved, set to ‘b000 if writing the register
3	WAIT	0	R/W	Set to 1 to enable the wait timer between data channel acquisitions
2	RSVD	0	R/W	Reserved, set to 0 if writing the register
1	CON	0	R/W	Set to 1 to enable data channel acquisitions
0	PON	0	R/W	Set to 1 if writing the register

The register 0xFA, bit 0 activates the internal oscillator for timer and ADC to operate. This bit should be not cleared for data conversion and acquisition. For the low power mode, this bit should be cleared.

Writing register 0xFA to 0x03 would active light engine to enable data acquisition. Writing register 0xFA to 0x83 would latch sensor data into the data registers.

Addr: 0xF8		INT_POLL_CLR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	RSVD	0	R/W	Reserved, set to ‘b00000 if writing the register
2	CLR	0	R/W	Set to 1 for asserted interrupt pin; Write 1 to clear it
1:0	RSVD	0	R/W	Reserved, set to ‘b00 if writing the register

The register 0xF8, bit 2 can be used for data valid or data ready purpose. This bit can be polled before issuing 0x83 to register 0xFA.

4.3.6 Data Register

Each channel data are two bytes in two registers using little endian. Both 0xDC/0xDD and 0xEC/0xED registers are shared with two channels each.

4.3.7 Low Power Mode

The sequence to configure AS726xN into low power mode

Write Register 0xFA to 0x00

Write register 0x73 to 0x02

The sequence to configure AS726xN out of low power mode

Write register 0x73 to 0x00

Wait for at least 50us

Write register 0xFA to 0x03

4.4 Two AS726xNs in Same I²C Bus

It is possible to connect two AS726xNs into the same system. For example, you could connect two AS7261Ns into the same system or one AS7262N with one AS7263N into the same system for more channels spectrometer.

In order to support two sensors, we will control RESN to initialize the sensors separately. Please configure hardware connection as below.

1. Connect RESN (pin 2) of one AS726xN to a microcontroller;
2. Pull the RESN of another AS726xN to power via a pull up resistor.

We initialize the sensor with RESN connected to power first and change the slave address to 0x59. Then initialize another sensor with slave address 0x49.

After power up or reset, put the RESN low and program the following registers to the slave address 0x49

Write 0x8A to Reg 0x70;

Write 0x02 to Reg 0x71;

Write 0x02 to Reg 0xB0;

Write 0x00 to Reg 0x88;

Write 0x 06 to Reg 0x9A; (This configures the device slave address into 0x59.)

Then pull the RESN to HIGH and program the following registers to the slave address 0x49.

Write 0x8A to Reg 0x70;

Write 0x02 to Reg 0x71;

Write 0x02 to Reg 0xB0;

Write 0x00 to Reg 0x88;

Write 0x02 to Reg 0x9A;

The device with controlled RESN has the slave address 0x49 and the other has 0x59. Both devices are ready to work now.

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7 Revision Information

Changes from previous version to current revision 1-01 (2017-Apr-18)	Page
Updated Programming Sequence	7-10
Updated Light Source	4

Note: Page numbers for the previous version may differ from page numbers in the current revision.
Correction of typographical errors is not explicitly mentioned.