AS72651

Smart 6-Channel NIR *Spectral_ID* Sensor with Electronic Shutter and 18-Channel AS7265x Master Capability

General Description

The AS72651 is a digital 6-channel multi-spectral sensor for spectral identification in the near IR light wavelengths, serving as master controller for the AS7265x chip-set. It has 6 independent on-device optical filters whose spectral response is defined in the NIR wavelengths from 600nm to 870nm with FWHM of 20nm. The AS72651, combined with the AS72652 (spectral response from 560nm to 940nm) and the AS72653 (spectral response from 410nm to 535nm) form an AS7265x 18-channel multi-spectral sensor chip-set from 410nm to 940nm.

Each AS7265x device has two integrated LED drivers with programmable current and can be timed for electronic shutter applications.

The device family integrates Gaussian filters into standard CMOS silicon via nano-optic deposited interference filter technology in LGA packages that also provide built-in apertures to control the light entering the sensor array.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS72651, Smart 6-Channel NIR Spectral_ID Sensor with Electronic Shutter and 18-Channel AS7265x Master Capability are listed below:

Figure 1:
AS7265x Chip-Set Benefits and Features

Benefits	Features
• Compact 18-channel spectrometry chip-set solution	• Master device for 3 chip set delivering 18 visible and NIR channels from 410nm to 940nm each with 20nm FWHM
	• UART or I^2C slave digital Interface
	• Visible filter set realized by silicon interference filters
• No additional signal conditioning required	• 16-bit ADC with digital access
	• Programmable LED drivers
	• 2.7V to 3.6V with I^2C interface

Benefits	Features
• Small, robust package, with built-in aperture	• 20-pin LGA package 4.5mm x 4.7mm x 2.5mm -40°C to 85°C temperature range

Applications

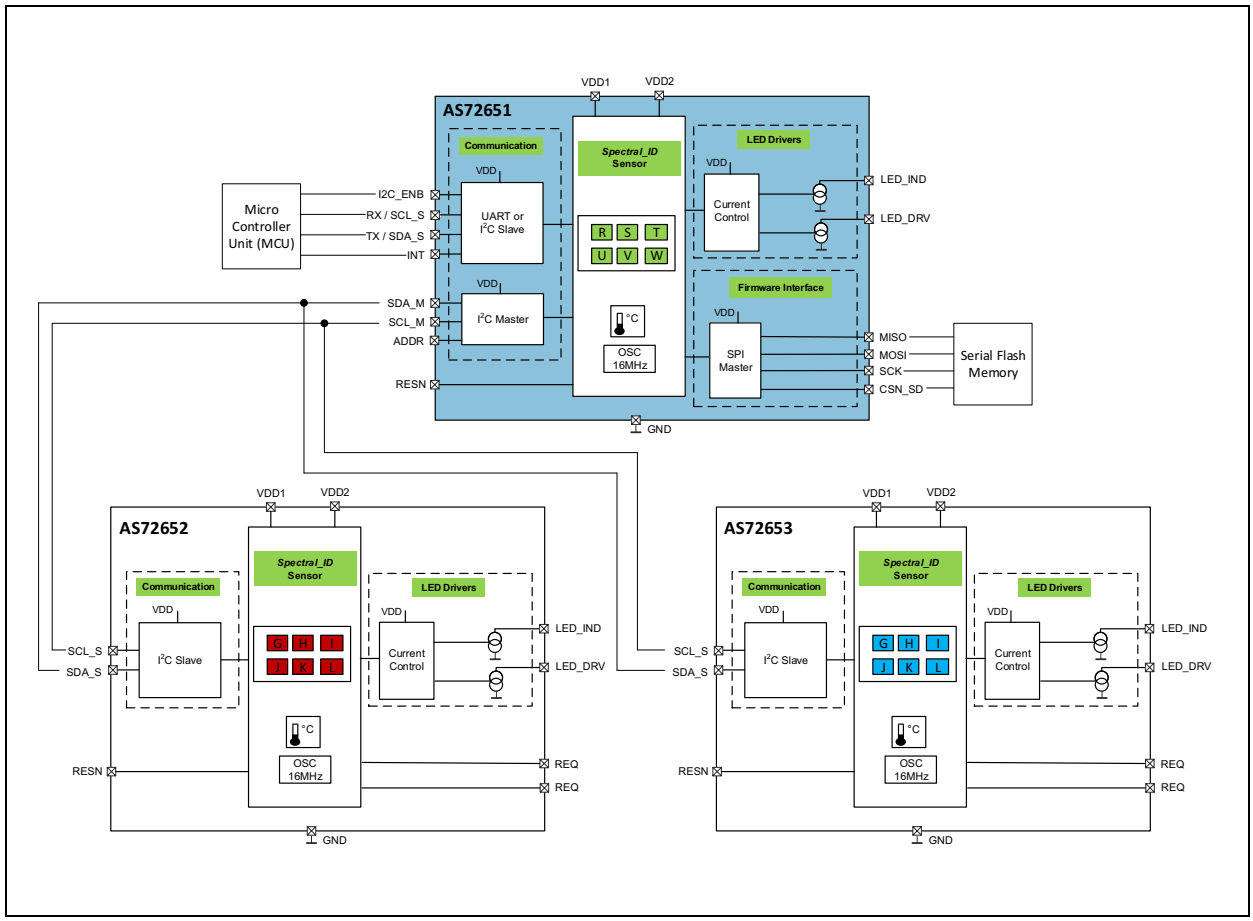
The AS72651 applications include:

- Product/Brand authentication
- Anti-counterfeiting
- Portable spectroscopy
- Product safety/adulteration detection
- Horticultural and specialty lighting
- Material analysis

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS7265x Chip-Set Block Diagram



Note(s):

1. Refer to the Application Diagram in Figure 52.

Pin Assignments

The device pin assignments are described below.

Figure 3:
Pin Diagram of AS72651 (Top View)

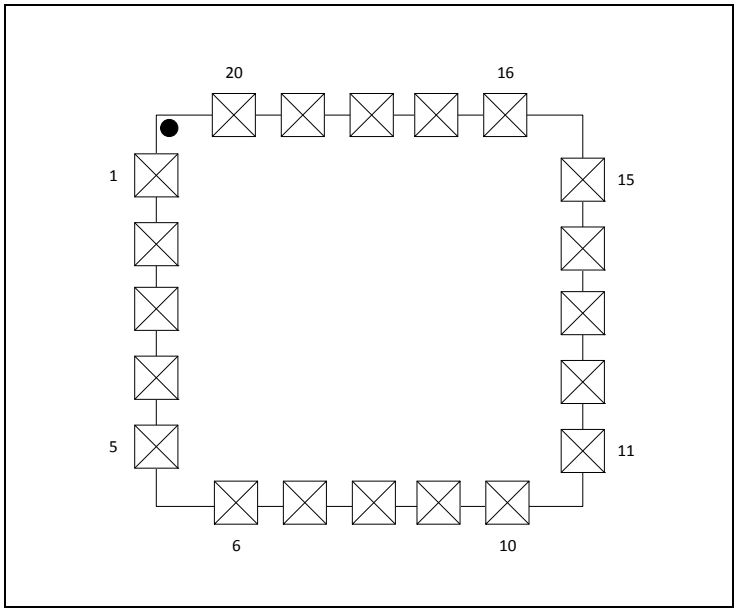


Figure 4:
AS72651 Pin Description

Pin No.	Pin Name	Pin Type	Description
1	SDA_M	Digital Input and Output	I^2C master data for communicating with AS72652 and AS72653
2	RESN	Digital Input	Reset pin, active low (w/internal pull-up to VDD)
3	SCK	Digital Output	SPI serial clock
4	MOSI	Digital Input and Output	SPI MOSI
5	MISO	Digital Input and Output	SPI MISO
6	CSN_EE	Digital Output	Chip select for external EEPROM, active low
7	CSN_SD	Digital Output	Chip select for SD card interface, active low
8	I2C_ENB	Digital Input	Selects UART (low) or I^2C (high) operation
9	INT	Digital Output (open drain)	INT is active low
10	NC		Not functional. No connect

Pin No.	Pin Name	Pin Type	Description
11	RX / SCL_S	Digital Input	RX (UART) or SCL_S (I^2C slave) depending on I2C_ENB setting
12	TX / SDA_S	Digital Input and Output	TX (UART) or SDA_S (I^2C slave) depending on I2C_ENB setting
13	ADDR	Digital Output (open drain)	Sets address for AS72653
14	VDD2	Voltage Supply	Voltage supply
15	LED_DRV	Analog Output	LED driver output for driver LED, current sink
16	GND	Supply	Ground
17	VDD1	Voltage Supply	Voltage supply
18	LED_IND	Analog Output	LED driver output for indicator LED, current sink
19	NC		Not functional. No connect
20	SCL_M	Digital Output	I^2C master clock for communicating with AS72652 and AS72653

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings of AS72651 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device is not designed for high energy UV (ultraviolet) environments, including upward looking outdoor applications, which could affect long term optical performance.

Figure 5:
Absolute Maximum Ratings of AS72651

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{DD1_MAX}	Supply Voltage VDD1	-0.3	5	V	Pin VDD1 to GND
V_{DD2_MAX}	Supply Voltage VDD2	-0.3	5	V	Pin VDD2 to GND
V_{DD_IO}	Input/Output Pin Voltage	-0.3	VDD+0.3	V	Input/Output Pin to GND
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	JESD78D
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	±1000		V	JS-001-2014
ESD_{CDM}	Electrostatic Discharge CDM	±500		V	JESD22-C101F
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a 168 hour max. floor lifetime

Electrical Characteristics

All limits are guaranteed with VDD = VDD1 = VDD2 = 3.3V, T_{AMB} = 25°C. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

VDD1 and VDD2 should be sourced from the same power supply output.

Figure 6:
Electrical Characteristics of AS72651

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General Operating Conditions						
VDD1 /VDD2	Voltage Operating Supply	UART Interface	2.97	3.3	3.6	V
VDD1 /VDD2	Voltage Operating Supply	I^2C Interface	2.7	3.3	3.6	V
T_{AMB}	Operating Temperature		-40	25	85	°C
I_{VDD}	Operating Current				5	mA
Internal RC Oscillator						
F_{OSC}	Internal RC Oscillator Frequency		15.7	16	16.3	MHz
t_{JITTER} (1)	Internal Clock Jitter	@25°C			1.2	ns
Temperature Sensor						
D_{TEMP}	Absolute Accuracy of the Internal Temperature Measurement		-8.5		8.5	°C
Indicator LED						
I_{IND}	LED Current		1		8	mA
I_{ACC}	Accuracy of Current		-30		30	%
V_{LED}	Voltage Range of Connected LED	Vds of current sink	0.3		VDD	V
LED_DRV						
I_{LED1}	LED Current		12.5		100	mA
I_{ACC}	Accuracy of Current		-10		10	%
V_{LED}	Voltage Range of Connected LED	Vds of current sink	0.3		VDD	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital Inputs and Outputs						
I_{IH}, I_{IL}	Logic Input Current	Vin=0V or VDD	-1		1	µA
V_{IH}	CMOS Logic High Input		0.7* VDD		VDD	V
V_{IL}	CMOS Logic Low Input		0		0.3* VDD	V
V_{OH}	CMOS Logic High Output	I=1mA			VDD-0.4	V
V_{OL}	CMOS Logic Low Output	I=1mA			0.4	V
t_{RISE} (1)	Current Rise Time	C(Pad)=30pF			5	ns
t_{FALL} (1)	Current Fall Time	C(Pad)=30pF			5	ns

Note(s):

1. Guaranteed, not tested in production.

Timing Characteristics

Figure 7:
AS72651 I²C Slave Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C Interface						
f_{SCLK}	SCL Clock Frequency		0		400	kHz
t_{BUF}	Bus Free Time Between a STOP and START		1.3			µs
$t_{HS:STA}$	Hold Time (Repeated) START		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START		0.6			µs
$t_{HS:DAT}$	Data Hold Time		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time		100			ns
t_R	Rise Time of Both SDA and SCL		20		300	ns
t_F	Fall Time of Both SDA and SCL		20		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	CB - total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

Figure 8:
I²C Slave Timing Diagram

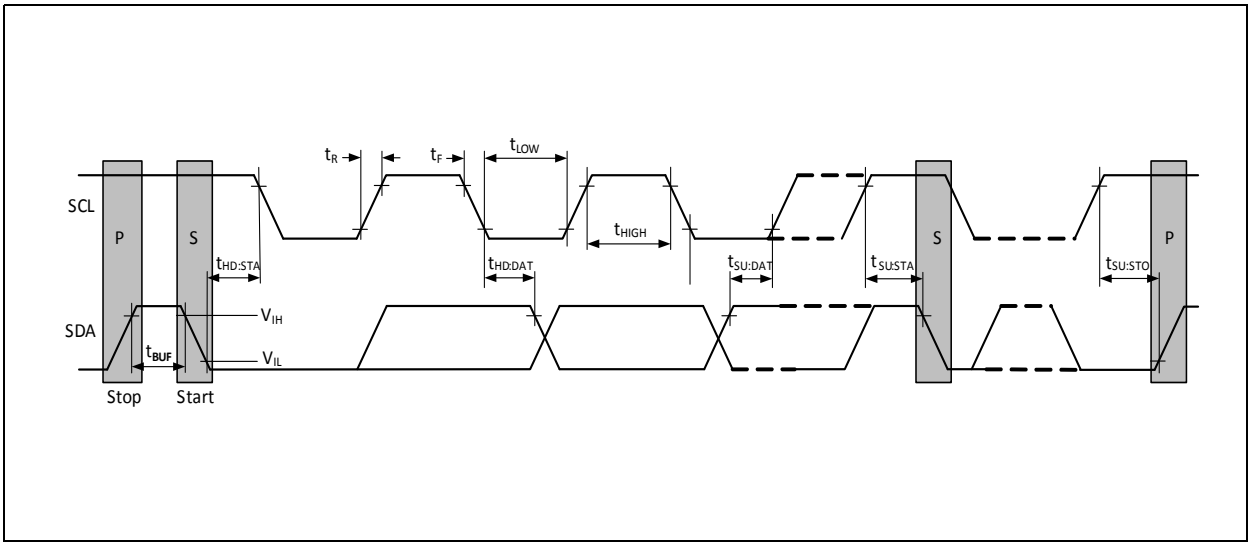


Figure 9:
AS72651 SPI Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI Interface						
f_{SCK}	Clock Frequency		0		16	MHz
t_{SCK_H}	Clock High Time		40			ns
t_{SCK_L}	Clock Low Time		40			ns
t_{SCK_RISE}	SCK Rise Time		5			ns
t_{SCK_FALL}	SCK Fall Time		5			ns
t_{CSN_S}	CSN Setup Time	Time between CSN high-low transition to first SCK high transition	50			ns
t_{CSN_H}	CSN Hold Time	Time between last SCK falling edge and CSN low-high transition	100			ns
t_{CSN_DIS}	CSN Disable Time		100			ns
t_{DO_S}	Data-Out Setup Time		5			ns
t_{DO_H}	Data-Out Hold Time		5			ns
t_{DI_V}	Data-In Valid		10			ns

Figure 10:
SPI Master Write Timing Diagram

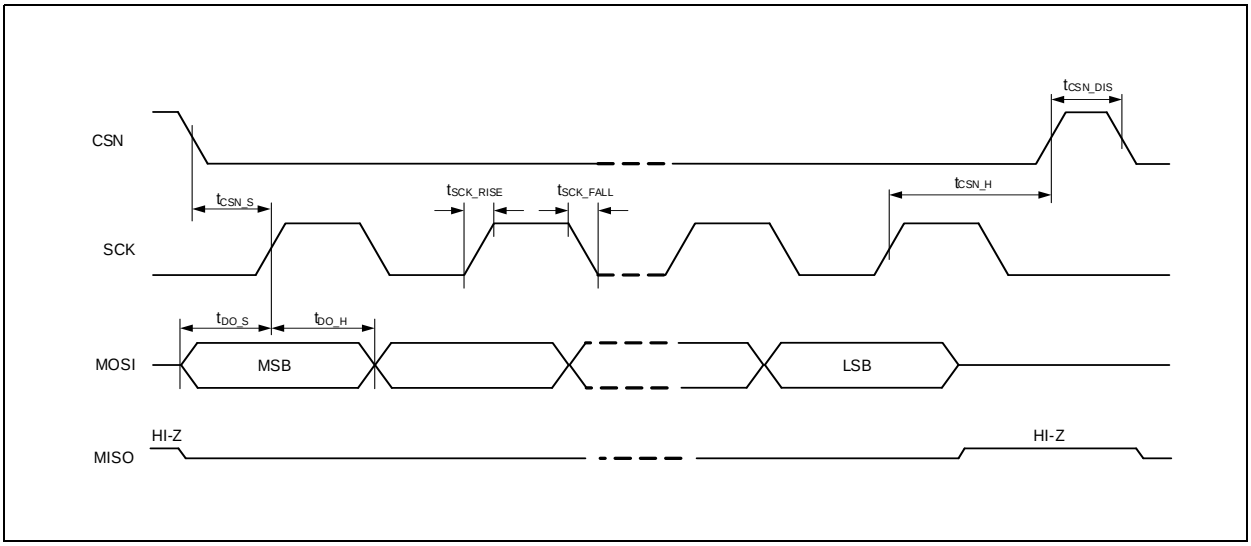
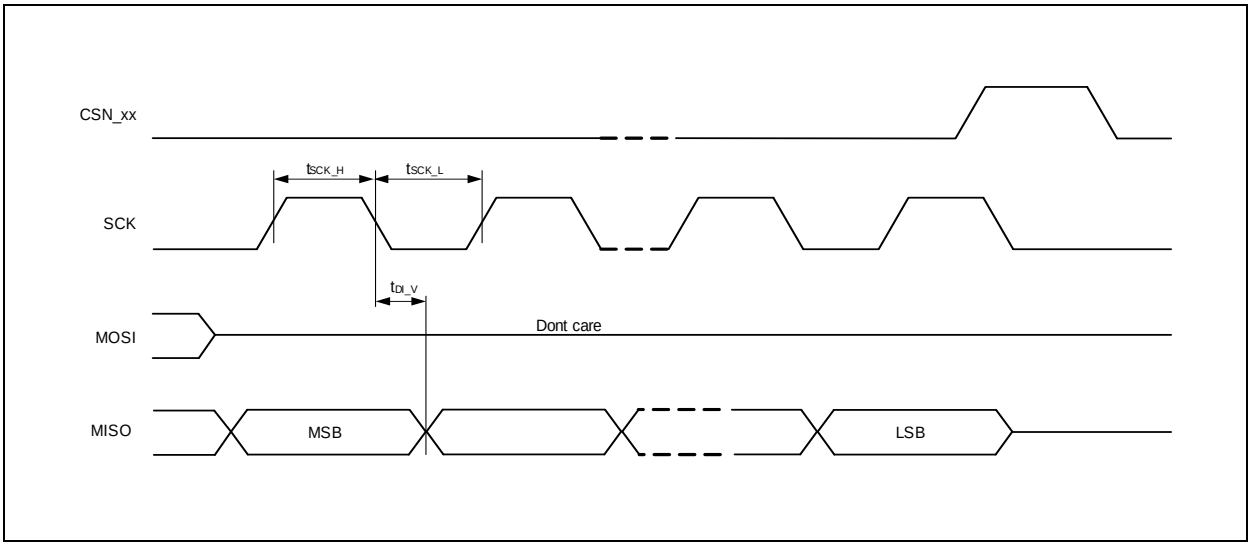


Figure 11:
SPI Master Read Timing Diagram



Typical Operating Characteristics

Optical Characteristics

All optical characteristics are optimized for diffused light.

Figure 12:
AS7265x 18-Channel Spectral Responsivity

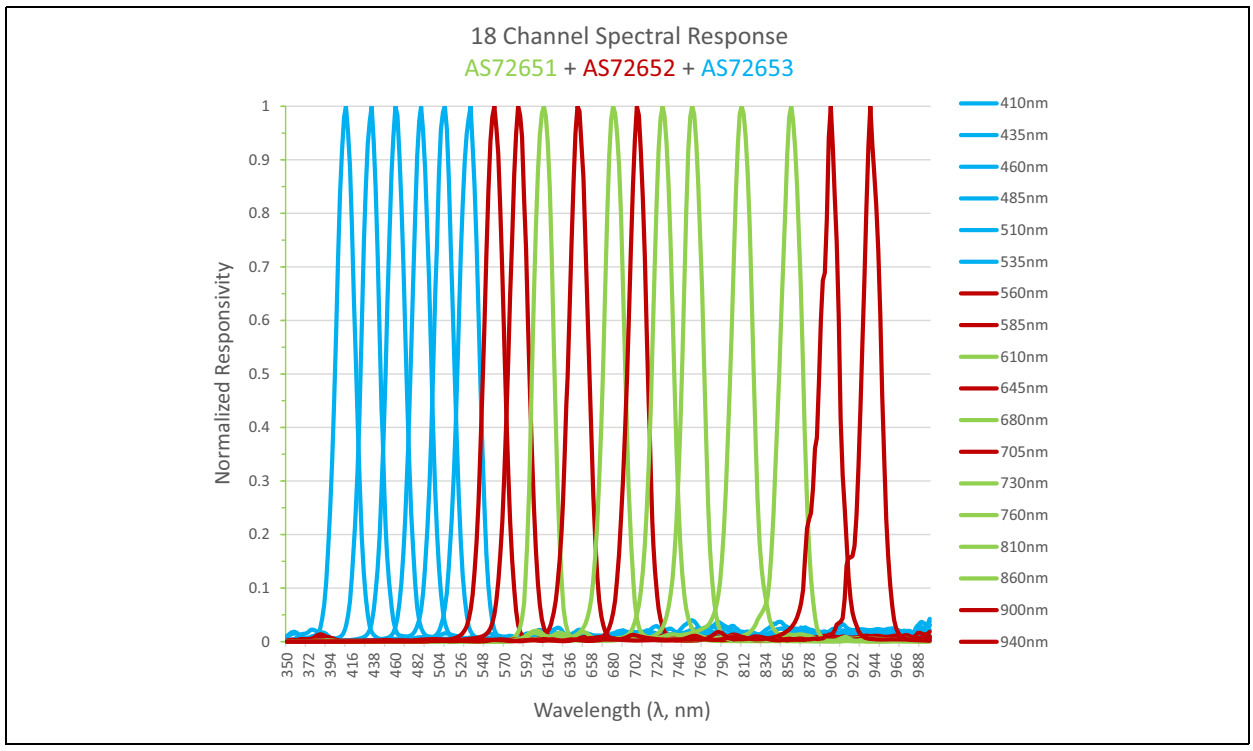


Figure 13:
AS72651 Spectral Responsivity

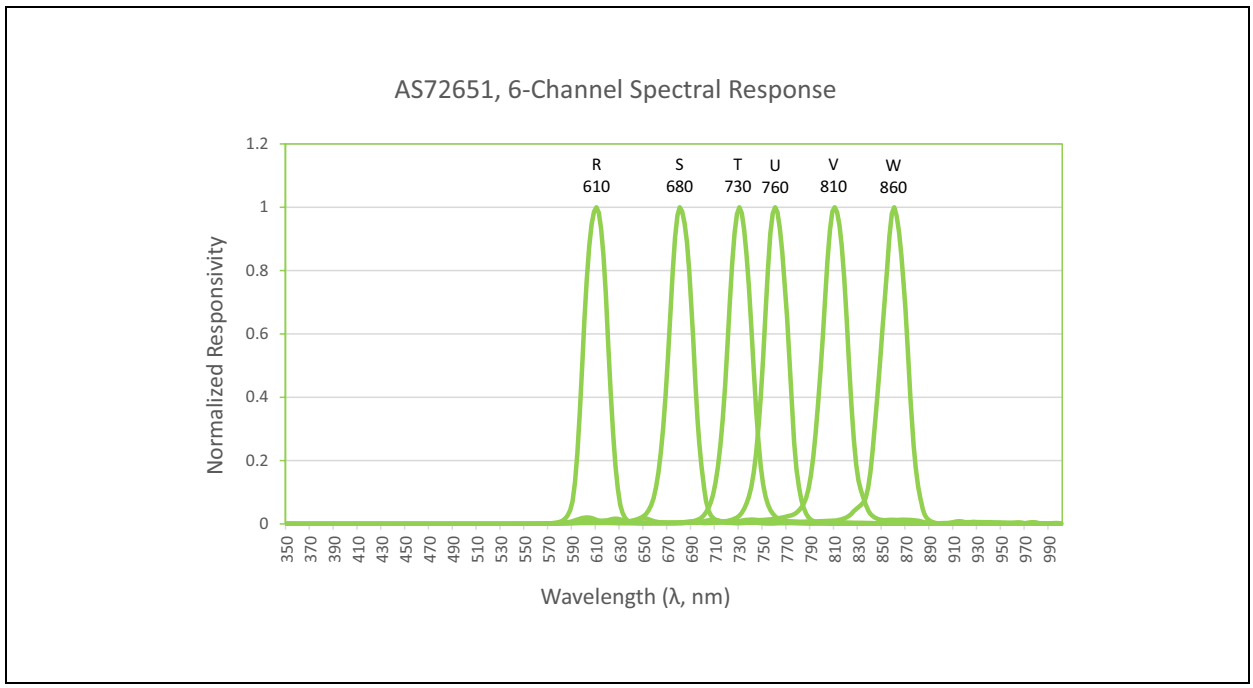


Figure 14:
Optical Characteristics of AS72651 (Pass Band) (1)

Symbol	Parameter	Test Conditions	Channel (nm)	Min	Typ	Max	Unit
R	Channel R	Incandescent(2),(4)	610		35(3),(4)		counts/ (µW/cm^2)
S	Channel S	Incandescent(2),(4)	680		35(3),(4)		counts/ (µW/cm^2)
T	Channel T	Incandescent(2),(4)	730		35(3),(4)		counts/ (µW/cm^2)
U	Channel U	Incandescent(2),(4)	760		35(3),(4)		counts/ (µW/cm^2)
V	Channel V	Incandescent(2),(4)	810		35(3),(4)		counts/ (µW/cm^2)
W	Channel W	Incandescent(2),(4)	860		35(3),(4)		counts/ (µW/cm^2)
FWHM	Full Width Half Max		20		20		nm
Wacc	Wavelength Accuracy				±10		nm
dark	Dark Channel Counts	GAIN=64, T_{AMB}=25°C				5	counts
AFOV	Average Field of View				±20.5		deg

Note(s):

1. Calibration and measurements are made using diffused light.
2. Each channel is tested with GAIN = 16x, Integration Time (INT_T) = 166ms and VDD = VDD1 = VDD2 = 3.3V, T_{AMB}=25°C.
3. The accuracy of the channel counts/µW/cm^2 is ±12%.
4. The light source is an incandescent light with an irradiance of ~1500µW/cm^2 (300-1000nm). The energy at each channel (R, S, T, U, V, W) is calculated with a ±33nm bandwidth around the center wavelengths (610, 680, 730, 760, 810, 860nm).

Figure 15:
AS72652 Spectral Responsivity

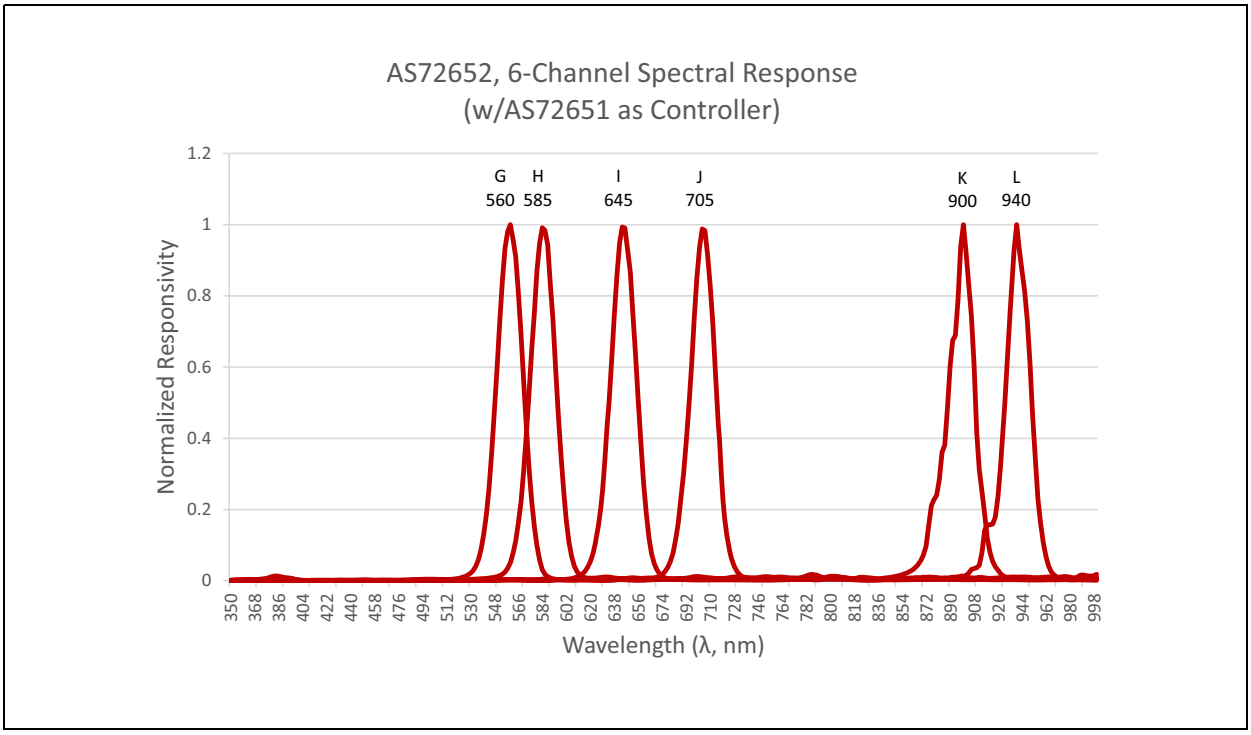


Figure 16:
Optical Characteristics of AS72652 (Pass Band) (1)

Symbol	Parameter	Conditions	Channel (nm)	Min	Typ	Max	Unit
G	Channel G	3300K White LED(2)	560		35		counts/ (µW/cm^2)
H	Channel H	3300K White LED(2)	585		35		counts/ (µW/cm^2)
I	Channel I	3300K White LED(2)	645		35		counts/ (µW/cm^2)
J	Channel J	3300K White LED(2)	705		35		counts/ (µW/cm^2)
K	Channel K	Incandescent(2)	900		35		counts/ (µW/cm^2)
L	Channel L	940nm LED	940		35		counts/ (µW/cm^2)
FWHM	Full Width Half Max		20		20		nm

Symbol	Parameter	Conditions	Channel (nm)	Min	Typ	Max	Unit
Wacc	Wavelength Accuracy				±10		nm
dark	Dark Channel Counts	GAIN=64, T_{AMB}=25°C				5	counts
AFOV	Average Field of View				±20.5		deg

Note(s):

1. Calibration and measurements are made using diffused light.
2. Each channel is tested with GAIN = 16x, Integration Time (INT_T) = 166ms and VDD = VDD1 = VDD2 = 3.3V, T_{AMB}=25°C.

Figure 17:
AS72653 Spectral Responsivity

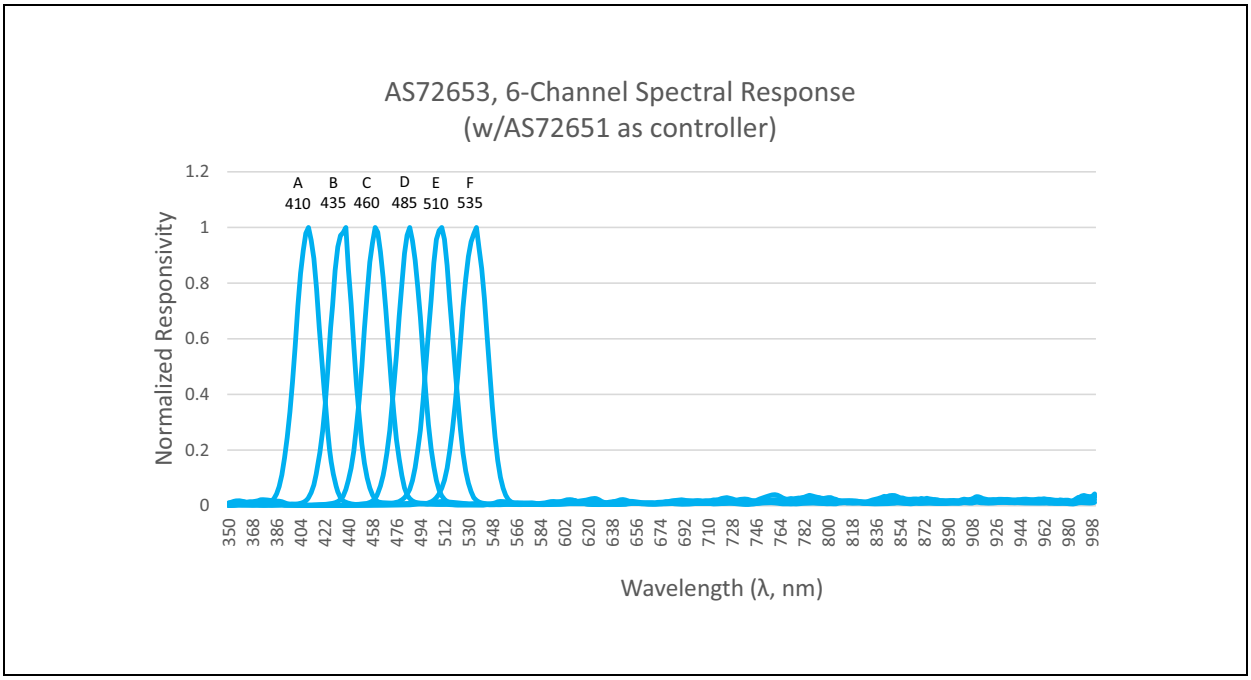


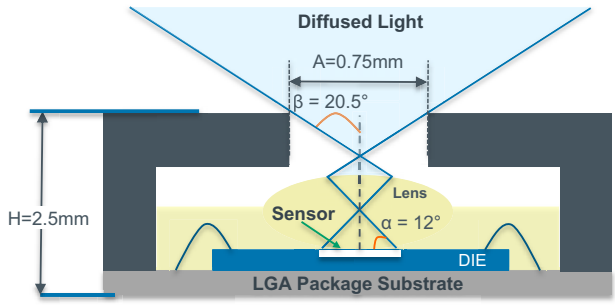
Figure 18:
Optical Characteristics of AS72653 (Pass Band)(1)

Symbol	Parameter	Conditions	Channel (nm)	Min	Typ	Max	Unit
A	Channel A	400nm LED(2)	410		35		counts/ ($\mu W/cm^2$)
B	Channel B	5700K White LED(2)	435		35		counts/ ($\mu W/cm^2$)
C	Channel C	5700K White LED(2)	460		35		counts/ ($\mu W/cm^2$)
D	Channel D	5700K White LED(2)	485		35		counts/ ($\mu W/cm^2$)
E	Channel E	5700K White LED(2)	510		35		counts/ ($\mu W/cm^2$)
F	Channel F	5700K White LED(2)	535		35		counts/ ($\mu W/cm^2$)
FWHM	Full Width Half Max		20		20		nm
Wacc	Wavelength Accuracy				±10		nm
dark	Dark Channel Counts	GAIN=64, T_{AMB}=25°C				5	counts
AFOV	Average Field of View				±20.5		deg

Note(s):

1. Calibration and measurements are made using diffused light.
2. Each channel is tested with GAIN = 16x, Integration Time (INT_T) = 166ms and VDD = VDD1 = VDD2 = 3.3V, T_{AMB}=25°C.

Figure 19:
AS72651, AS72652 and AS72653 LGA Average Field of View



Detailed Description

AS7265x 18 Channel *Spectral_ID* Detector Overview

Each of the three AS7265x *Spectral_ID* devices are next-generation digital 6-channel spectral sensor devices. Each of the 6-channels has a Gaussian filter characteristic with a full width half maximum (FWHM) bandwidth of 20nm. The filters use an interference topology design which enables temperature stability with minimal drift over time or temperature. Filter accuracy will be affected by the angle of incidence which itself is limited by integrated aperture and internal micro-lens structure. The aperture-limited average field of view is ±20.5° to deliver specified accuracy.

Each device contains an analog-to-digital converter (16-bit resolution ADC) which integrates the current from each channel's photodiode. Upon completion of the conversion cycle, the integrated result is transferred to the corresponding data registers. The transfers are double-buffered to ensure data integrity is maintained.

The external MCU interface control via I^2C registers or AT commands, transparently controls the AS72652 and/or AS72653.

A serial flash EPROM is a required operating companion for this device and enables factory calibration/normalization of the filters. Supported device types are noted in Ordering Information at the end of this document. Required operating code can be downloaded at download.ams.com.

Channel Data Conversion of the AS7265x Devices

All three of these 6-channels devices use conversion implemented via two photodiode banks in each device. Refer to the two figures below. Bank 1 consists of register data from 4 of the 6 photodiodes, with 2 registers zeroed and Bank 2 consists of data from a different set of 4 of the 6 photodiodes, with 2 different registers zeroed. Spectral conversion requires the integration time (IT in ms) set to complete. If both photodiode banks are required to complete the conversion, the 2^{nd} bank requires an additional IT ms. Minimum IT for a single bank conversion is 2.8 ms. If data is required from all 6 photodiodes then the device must perform 2 full conversions (2 x Integration Time).

This spectral data conversion process operates continuously, new data is available after each IT ms period.

The conversion process is controlled with BANK Mode settings in the AS72651 as follows:

BANK Mode 0 Registers:

AS72651 data will be in S, T, U & V registers (R & W will be zero)

AS72652 data will be in G, H, K & I registers (J & L will be zero)

AS72653 data will be in A, B, E & C registers (D & F will be zero)

BANK Mode 1 Registers:

AS72651 data will be in R, T, U & W registers (S & V will be zero)

AS72652 data will be in G, H, J & L registers (I & K will be zero)

AS72653 data will be in F, A, B & D registers (C & E will be zero)

BANK Mode 2 Registers:

AS72651 data will be in S, T, U, V, R & W registers

AS72652 data will be in G, H, K, I, J & L registers

AS72653 data will be in A, B, C, D, E & F registers

For BANK Mode 2, care should be taken to assure prompt interrupt servicing so integration values from both banks are all derived from the same spectral conversion cycle.

Figure 20:
AS7265x Photo Diode Arrays

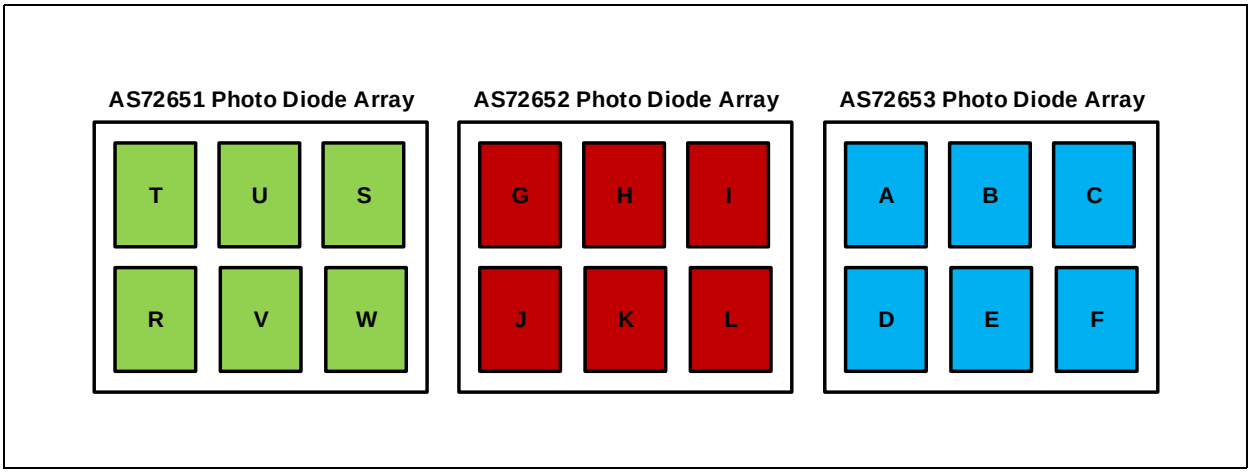
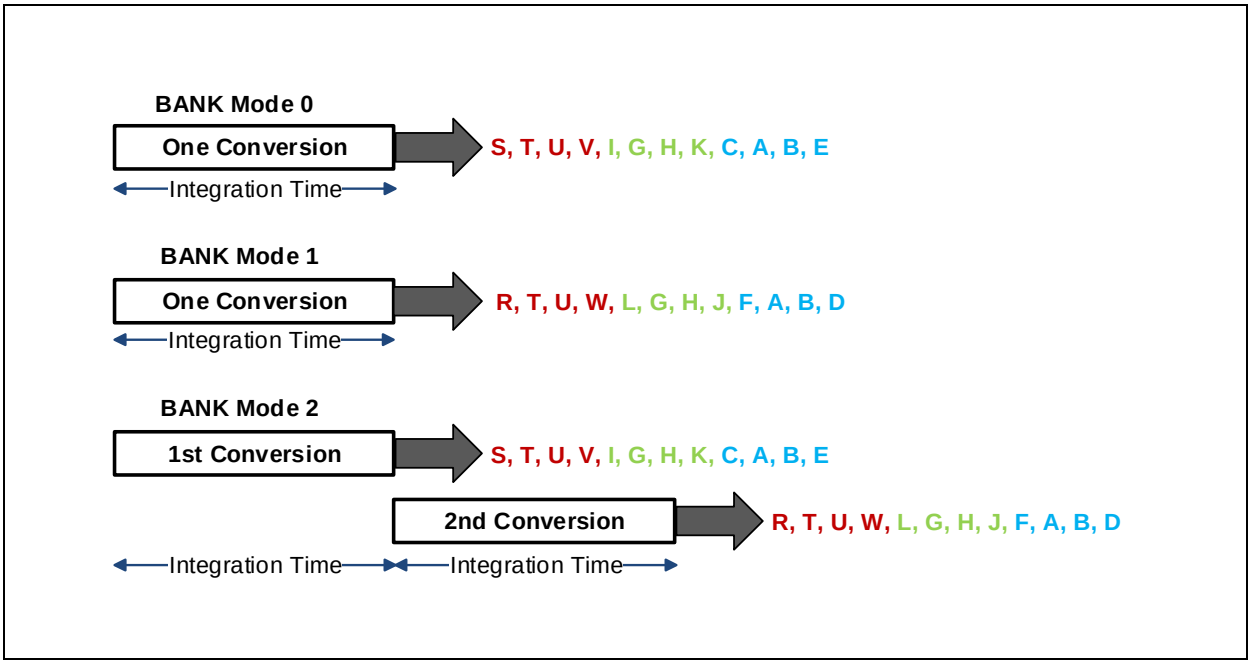


Figure 21:
Bank Mode and Data Conversion



RC Oscillator

The timing generation circuit consists of on-chip 16MHz, temperature compensated oscillators, which provide the individual master clocks of the AS7625x devices

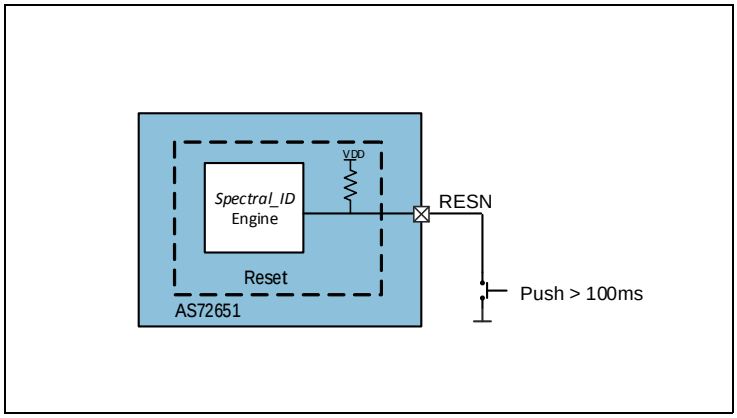
Temperature Sensor

The AS7265x internal temperature sensors are constantly measuring on-chip temperature to enable temperature compensation procedures, and can be read via I^2C registers or AT commands in the AS72651.

Reset

Pulling down the RESN pin for longer than 100ms resets the AS72651 which proceed to reset the AS72562 and the same RESN signal shown below can be used directly to reset the AS72653.

Figure 22:
Reset Circuit



AS7265x LED_IND Controls

There are LED_IND pins on all AS7265x devices. An LED connected to LED_IND can be used as a general power indicator and will automatically be used to indicate a Flash firmware update is occurring.

During a firmware update of the AS72651 via an external SD card the indicator LED starts flashing (500ms pulses). When programming is completed the device re-starts and the indicator LED stops flashing. The LED_IND can then be setup as needed. Each AS7265x LED_IND source can be turned on/off via AT commands or I^2C register control, and LED_IND sink current is programmable to 1mA, 2mA, 4mA or 8mA. This LED_IND control can also be used in applications just like the LED_DRV control (described below), if the lower current sink of the LED_IND control is appropriate.

Electronic Shutter with AS7265x LED_DRV Driver Control

There are LED_DRV pins on all AS7265x devices. The LED_DRV pin can be used to control external LED sources as needed for sensor applications. LED_DRV can sink a programmable current of 12.5mA, 25mA, 50mA or 100mA. The control can be turned on/off via I^2C registers or AT commands, and as such it provides the AS7265x device with an electronic shutter.

Interrupt Operation

Interrupt operation is only needed for AS72651 as it transparently controls data collection from the AS72652 (if used) or AS72653 (if used).

If BANK is set in the AS72651 to Mode 0 or Mode 1, data is ready after the 1st integration time. If BANK is set to Mode 2, data is ready after two integration times.

For interrupt operation using I²C registers, if interrupts are enabled and data is ready, the INT pin is set low and DATA_RDY is set to 1. The INT line is released (returns high) when the control register is read. DATA_RDY is cleared to 0 when any of the sensor registers are read. For multi-byte sensor data (2 or 4 bytes), after the 1st byte is read the remaining bytes are shadow protected in case an integration cycle completes just after the 1st byte is read. The sensors continue to gather information at the rate of the integration time, hence if the sensor registers are not read when the interrupt line goes low, it will stay low and the next cycle's sensor data will be available in the registers at the end of the next integration cycle.

For interrupt operation using AT Commands, if interrupts are enabled and data is ready the INT pin is set low and is released (returns high) after any sensor data is read.

Required Flash Memory

Serial flash EPROM is a required operating companion for this device, and enables the I²C and UART interfaces, as well as enabling calibrated data results. Supported device types are noted in Ordering Information at the end of this document. Required operating code can be downloaded at download.ams.com.

I²C Slave Interface

If selected by the I2C_ENB pin setting, interface and control can be accomplished through an I²C compatible slave interface to a set of registers that provide access to device control functions and output data. These registers on the AS72651 are, in reality, implemented as *virtual* registers in software. The actual I²C slave hardware registers number only three and are described in the table below. The steps necessary to access the virtual registers defined in the following are explained in pseudocode for external I²C master writes and reads below.

I²C Feature List

- Fast mode (400kHz) and standard mode (100kHz) support.
- 7+1-bit addressing mode.
- Write format: Byte.
- Read format: Byte.

- SDA input delay and SCL spike filtering by integrated RC-components.

Figure 23:
I²C Slave Device Address and Physical Registers

Entity	Description	Note
Device Slave Address	8-bit slave address	Byte = 1001001x (device address = 49 hex) • x= 1 for Master Read (byte = 93 hex) • x= 0 for Master Write (byte = 92 hex)
STATUS Register	I²C slave interface STATUS register. Read-only.	Register Address = 0x00 Bit 1: TX_VALID • 0 - New data may be written to WRITE register • 1 -WRITE register occupied. Do NOT write. Bit 0: RX_VALID • 0 -No data is ready to be read in READ register. • 1 -Data byte available in READ register.
WRITE Register	I²C slave interface WRITE register. Write-only.	Register Address = 0x01 • 8-Bits of data written by the I²C Master intended for receipt by the I²C slave. Used for both *virtual* register addresses and write data.
READ Register	I²C slave interface READ register. Read-only.	Register Address = 0x02 • 8-Bits of data to be read by the I²C Master.

I²C Virtual Register Write Access

I²C Virtual Resister Byte Write, detailed below, shows the pseudocode necessary to write virtual registers on the AS72651. Note that, because the actual registers of interest are realized as virtual registers, a means of indicating whether there is a pending read or write operation of a given virtual register is needed. To convey this information, the most significant bit of the virtual register address is used as a marker. If it is 1, then a write is pending, otherwise the slave is expecting a virtual read operation. The pseudocode illustrates the proper technique for polling of the I²C slave status register to ensure the slave is ready for each transaction.

I²C Virtual Register Byte Write

Pseudocode

Poll I²C slave STATUS register;

If TX_VALID bit is 0, a write can be performed on the interface;

Send a virtual register address and set the MSB of the register address to 1 to indicate the pending write;

Poll I²C slave STATUS register;

If TX_VALID bit is 0, the virtual register address for the write has been received and the data may now be written;

Write the data.

Sample Code:

```
#define I2C_AS72XX_SLAVE_STATUS_REG     0x00
#define I2C_AS72XX_SLAVE_WRITE_REG      0x01
#define I2C_AS72XX_SLAVE_READ_REG       0x02
#define I2C_AS72XX_SLAVE_TX_VALID       0x02
#define I2C_AS72XX_SLAVE_RX_VALID       0x01

void i2cm_AS72xx_write(uint8_t virtualReg, uint8_t d)
{
        volatile uint8_tstatus;

        while (1)
        {
                // Read slave I2C status to see if the write buffer is ready.
                status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG);

                if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                        // No inbound TX pending at slave.  Okay to write now.
                        break ;
        }
        // Send the virtual register address (setting bit 7 to indicate a pending write).
        i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, (virtualReg | 0x80)) ;

        while (1)
        {
                // Read the slave I2C status to see if the write buffer is ready.
                status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

                if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                        // No inbound TX pending at slave.  Okay to write data now.
                        break ;
        }
        // Send the data to complete the operation.
        i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, d) ;
}
```

I²C Virtual Register Read access

I²C Virtual Register Byte Read, detailed below, shows the pseudocode necessary to read virtual registers on the AS72651. Note that in this case, reading a virtual register, the register address is not modified.

I²C Virtual Register Byte Read

Pseudocode

```
Poll I²C slave STATUS register;
If TX_VALID bit is 0, the virtual register address for the read may be written;
Send a virtual register address;
Poll I²C slave STATUS register;
If RX_VALID bit is 1, the read data is ready;
Read the data.
```

Sample Code

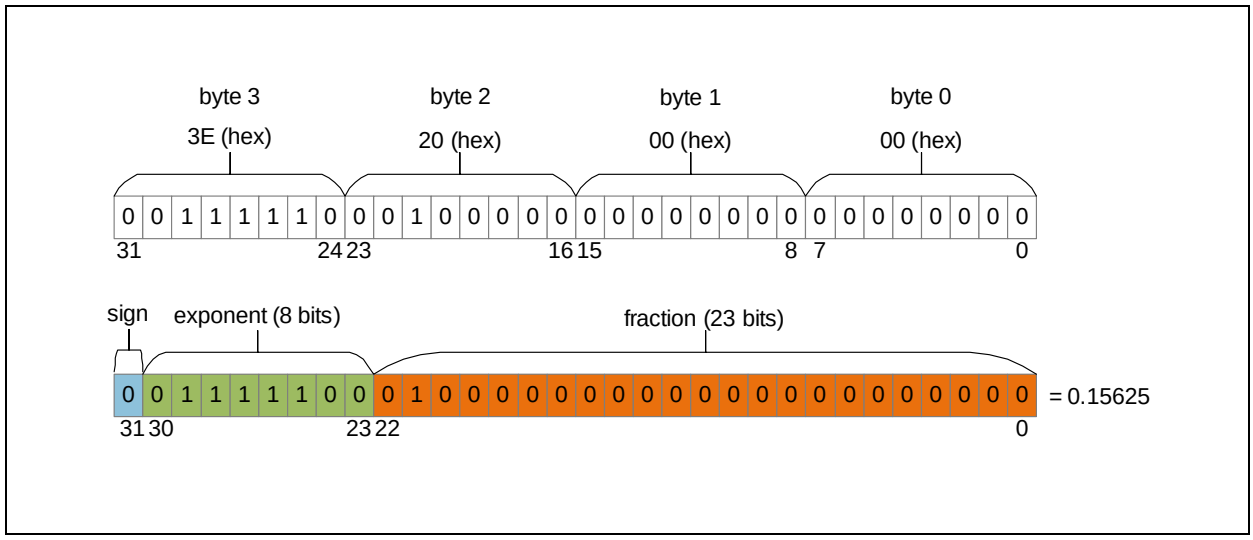
```
uint8_t i2cm_AS72xx_read(uint8_t virtualReg)
{
	volatile uint8_t status, d;

	while (1)
	{
		// Read slave I²C status to see if the read buffer is ready.
		status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

		if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
			// No inbound TX pending at slave. Okay to write now.
			break;
	}
	// Send the virtual register address (setting bit 7 to indicate a pending write).
	i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, virtualReg);

	while (1)
	{
		// Read the slave I²C status to see if our read data is available.
		status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG);

		if ((status & I2C_AS72XX_SLAVE_RX_VALID)!= 0)
			// Read data is ready.
			break;
	}
	// Read the data to complete the operation.
	d = i2cm_read(I2C_AS72XX_SLAVE_READ_REG) ;
	return d;s
}
```

The details of the i2cm_read() and i2cm_write() functions in previous figures are dependent upon the nature and implementation of the external I²C master device.

4-Byte Floating-Point (FP) Registers

Several 4 byte registers (hex) are used by the AS72651. Here is an example of how these registers are used to represent floating point data (based on the IEEE 754 standard).

Figure 24:
Example of the IEEE 754 Standard



The floating point (FP) value assumed by 32 bit **binary32 data** with a biased exponent **e** (the 8 bit unsigned integer) and a **23 bit fraction** is (for the above example):

(EQ1)

$$FPvalue = (-1)^{sign} \cdot \left(1 + \sum_{i-1}^{23} b_{23-i} \cdot 2^{-i}\right) \cdot 2^{(e-127)}$$

$$FPvalue = (-1)^{0} \cdot \left(1 + \sum_{i-1}^{23} b_{23-i} \cdot 2^{-i}\right) \cdot 2^{(124-127)}$$

$$FPvalue = 1 \cdot (1 + 2^{-2}) \cdot 2^{-3} = 0.15625$$

I²C Virtual Register Set

The figure below provides a summary of the AS72651 I²C register set for the AS72651 which serves as the master interface of the 3 device AS7265x set. Figures after that provide additional register details. All register data is hex, and all multi-byte entities are Big Endian (most significant byte is situated at the lowest register address).

Multiple byte registers (2 byte integer, or, 4 byte floating point) must be read in the order of ascending register addresses (low to high) and if capable of being written to, must also be written in the order ascending register addresses.

Figure 25:
AS72651 I²C Master Device Virtual Register Set Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Version Registers									
0x00: 0x01	AS72651_HW_ Version	AS72651 Hardware Version							
0x02: 0x03	AS72652_HW_ Version	AS72652 Hardware Version							
0x04: 0x05	AS72653_HW_ Version	AS72653 Hardware Version							
0x06: 0x07	AS72651_FW_ Version	AS72651 Firmware Version							
Control Registers									
0x0C/ 0x8C	Control_Setup	RST	INT	GAIN		Bank		DATA_ RDY	RSVD
0x0F/ 0x8F	INT_T	Integration Time							
0x12	AS72651_ Device_Temp	AS72651 Internal Device Temperature							
0x13	AS72652_ Device_Temp	AS72652 Internal Device Temperature							
0x14	AS72653_ Device_Temp	AS72653 Internal Device Temperature							
0x15/ 0x95	AS72651_LED_ Control	RSVD		ICL_DRV		LED DRV	ICL_IND		LED_IND
0x16/ 0x96	AS72652_LED_ Control	RSVD		ICL_DRV		LED DRV	ICL_IND		LED_IND
0x17/ 0x97	AS72653_LED_ Control	RSVD		ICL_DRV		LED DRV	ICL_IND		LED_IND
0x3F: 0xBF	I2C_CAL_SEL	RSVD						Value	

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Sensor Raw Data Registers (from the AS72651)									
0x18	R_High	Channel R High Data Byte							
0x19	R_Low	Channel R Low Data Byte							
0x1A	S_High	Channel S High Data Byte							
0x1B	S_Low	Channel S Low Data Byte							
0x1C	T_High	Channel T High Data Byte							
0x1D	T_Low	Channel T Low Data Byte							
0x1E	U_High	Channel U High Data Byte							
0x1F	U_Low	Channel U Low Data Byte							
0x20	V_High	Channel V High Data Byte							
0x21	V_Low	Channel V Low Data Byte							
0x22	W_High	Channel W High Data Byte							
0x23	W_Low	Channel W Low Data Byte							
Sensor Calibrated Data Registers (From the AS72651. Before reading set I2C_CAL_SEL=0x00)									
0x40: 0x43	R_Cal	Channel R Calibrated Data (floating point)							
0x44: 0x47	S_Cal	Channel S Calibrated Data (floating point)							
0x48: 0x4B	T_Cal	Channel T Calibrated Data (floating point)							
0x4C: 0x4F	U_Cal	Channel U Calibrated Data (floating point)							
0x50: 0x53	V_Cal	Channel V Calibrated Data (floating point)							
0x54: 0x57	W_Cal	Channel W Calibrated Data (floating point)							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Sensor Raw Data Registers (from the AS72652)									
0x24	G_High	Channel G High Data Byte							
0x25	G_Low	Channel G Low Data Byte							
0x26	H_High	Channel H High Data Byte							
0x27	H_Low	Channel H Low Data Byte							
0x28	I_High	Channel I High Data Byte							
0x29	I_Low	Channel I Low Data Byte							
0x2A	J_High	Channel J High Data Byte							
0x2B	J_Low	Channel J Low Data Byte							
0x2C	K_High	Channel K High Data Byte							
0x2D	K_Low	Channel K Low Data Byte							
0x2E	L_High	Channel L High Data Byte							
0x2F	L_Low	Channel L Low Data Byte							
Sensor Calibrated Data Registers (From the AS72652. Before reading set I2C_CAL_SEL=0x01)									
0x40: 0x43	G_Cal	Channel G Calibrated Data (floating point)							
0x44: 0x47	H_Cal	Channel H Calibrated Data (floating point)							
0x48: 0x4B	I_Cal	Channel I Calibrated Data (floating point)							
0x4C: 0x4F	J_Cal	Channel J Calibrated Data (floating point)							
0x50: 0x53	K_Cal	Channel K Calibrated Data (floating point)							
0x54: 0x57	L_Cal	Channel L Calibrated Data (floating point)							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Sensor Raw Data Registers (from the AS72653)									
0x30	A_High	Channel A High Data Byte							
0x31	A_Low	Channel A Low Data Byte							
0x32	B_High	Channel B High Data Byte							
0x33	B_Low	Channel B Low Data Byte							
0x34	C_High	Channel C High Data Byte							
0x35	C_Low	Channel C Low Data Byte							
0x36	D_High	Channel D High Data Byte							
0x37	D_Low	Channel D Low Data Byte							
0x38	E_High	Channel E High Data Byte							
0x39	E_Low	Channel E Low Data Byte							
0x3A	F_High	Channel F High Data Byte							
0x3B	F_Low	Channel F Low Data Byte							
Sensor Calibrated Data Registers (From the AS72653. Before reading set I2C_CAL_SEL=0x02)									
0x40: 0x43	A_Cal	Channel A Calibrated Data (floating point)							
0x44: 0x47	B_Cal	Channel B Calibrated Data (floating point)							
0x48: 0x4B	C_Cal	Channel C Calibrated Data (floating point)							
0x4C: 0x4F	D_Cal	Channel D Calibrated Data (floating point)							
0x50: 0x53	E_Cal	Channel E Calibrated Data (floating point)							
0x54: 0x57	F_Cal	Channel F Calibrated Data (floating point)							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Firmware Update Registers									
0x60/ 0xE0	FW_UPDATE_ CONTROL	Firmware Update Control							
0x61/ 0xE1	FWBC_HIGH	Firmware Byte Count, High Byte							
0x62/ 0xE2	FWBC_HIGH	Firmware Byte Count, Low Byte							
0x63/ 0xE3	FWLOAD	Firmware Download							

Detailed Register Descriptions

Figure 26:
AS72651 HW Version Registers

Addr: 0x00		AS72651_HW_Version		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Device Type		R	Device type number
Addr: 0x01		**AS72651_HW_Version**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	HW Version		R	Hardware version

Figure 27:
AS72652 HW Version Registers

Addr: 0x02		AS72652_HW_Version		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Device Type		R	Device type number
Addr: 0x03		**AS72652_HW_Version**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	HW Version		R	Hardware version

Figure 28:
AS72653 HW Version Registers

Addr: 0x04		AS72653_HW_Version		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Device Type		R	Device type number
Addr: 0x05		**AS72653_HW_Version**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	HW Version		R	Hardware version

Figure 29:
AS72651 FW Version Registers

Addr: 0x06		AS72651_FW_Version		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Minor Version		R	Minor version [1:0]
5:0	Sub Version		R	Sub version
Addr: 0x07		**AS72651_FW_Version**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Major Version		R	Major version
3:0	Minor Version		R	Minor version [5:2]

Figure 30:
Control Setup Register

Addr: 0x0C/0x8C		Control_Setup		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	RST	0	R/W	Set to 1 for soft reset, goes to 0 automatically after the reset
6	INT	0	R/W	Enable interrupt pin output (INT), 1: Enable, 0: Disable
5:4	GAIN	0	R/W	Sensor channel gain setting (all channels) ‘b00=1x; ‘b01=3.7x; ‘b10=16x; ‘b11=64x;
3:2	BANK	10	R/W	Data conversion type (continuous) ‘b00=Mode 0; ‘b01=Mode 1; ‘b10=Mode 2; ‘b11= reserved
1	DATA_RDY	0	R/W	1: Data ready to read, sets INT active if interrupt is enabled. Can be polled if not using INT.
0	RSVD	0	R	Reserved. Unused

Figure 31:
Integration Time Register

Addr: 0x0F/0x8F		INT_T		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	INT_T	0xFF	R/W	Integration time = <value> * 2.8ms (applies to all channels)

Figure 32:
AS72651 Device Temperature Register

Addr: 0x12		AS72651_Device_Temp		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Device_Temp		R	Device temperature data byte (°C)

Figure 33:
AS72652 Device Temperature Register

Addr: 0x13		AS72652_Device_Temp		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Device_Temp		R	Device temperature data byte (°C)

Figure 34:
AS72653 Device Temperature Register

Addr: 0x14		AS72653_Device_Temp		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Device_Temp		R	Device temperature data byte (°C)

Figure 35:
AS72651 LED Control Register

Addr: 0x15/0x95		AS72651_LED Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	RSVD	0	R	Reserved
5:4	ICL_DRV	00	R/W	LED_DRV current limit 'b00=12.5mA; 'b01=25mA; 'b10=50mA; 'b11=100mA;
3	LED_DRV	0	R/W	Enable LED_DRV 1: Enabled; 0: Disabled
2:1	ICL_IND	00	R/W	LED_IND current limit 'b00=1mA; 'b01=2mA; 'b10=4mA; 'b11=8mA;
0	LED_IND	0	R/W	Enable LED_IND 1: Enabled; 0: Disabled

Figure 36:
AS72652 LED Control Register

Addr: 0x16/0x96		AS72652_LED Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	RSVD	0	R	Reserved
5:4	ICL_DRV	00	R/W	LED_DRV current limit 'b00=12.5mA; 'b01=25mA; 'b10=50mA; 'b11=100mA;
3	LED_DRV	0	R/W	Enable LED_DRV 1: Enabled; 0: Disabled
2:1	ICL_IND	00	R/W	LED_IND current limit 'b00=1mA; 'b01=2mA; 'b10=4mA; 'b11=8mA;
0	LED_IND	0	R/W	Enable LED_IND 1: Enabled; 0: Disabled

Figure 37:
AS72653 LED Control Register

Addr: 0x17/0x97		AS72653_LED Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	RSVD	0	R	Reserved
5:4	ICL_DRV	00	R/W	LED_DRV current limit 'b00=12.5mA; 'b01=25mA; 'b10=50mA; 'b11=100mA;
3	LED_DRV	0	R/W	Enable LED_DRV 1: Enabled; 0: Disabled
2:1	ICL_IND	00	R/W	LED_IND current limit 'b00=1mA; 'b01=2mA; 'b10=4mA; 'b11=8mA;
0	LED_IND	0	R/W	Enable LED_IND 1: Enabled; 0: Disabled

Figure 38:
I²C Calibration Select Register

Addr: 0x3F/0xBF		I2C_Calibration_Select		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	RSVD			Reserved, do not use.
1:0	SEL_VALUE	00	R/W	Used to access the calibrated data values. Set to one of these values before reading the Calibrated Data from the selected device: 00=AS72651, 01=AS72652, 10=AS72652, 11=reserved, do not use.

Figure 39:
AS72651 Sensor Raw Data Registers

Addr: 0x18		R_High		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	R_High		R	Channel R High Data Byte
Addr: 0x19		**R_Low**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	R_Low		R	Channel R Low Data Byte
Addr: 0x1A		**S_High**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	S_High		R	Channel S High Data Byte
Addr: 0x1B		**S_Low**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	S_Low		R	Channel S Low Data Byte
Addr: 0x1C		**T_High**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	T_High		R	Channel T High Data Byte
Addr: 0x1D		**T_Low**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	T_Low		R	Channel T Low Data Byte
Addr: 0x1E		**U_High**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	U_High		R	Channel U High Data Byte
Addr: 0x1F		**U_Low**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	U_Low		R	Channel U Low Data Byte

Addr: 0x20		V_High		
Bit	Bit Name	Default	Access	Bit Description
7:0	V_High		R	Channel V High Data Byte
Addr: 0x21		V_Low		
Bit	Bit Name	Default	Access	Bit Description
7:0	V_Low		R	Channel V Low Data Byte
Addr: 0x22		W_High		
Bit	Bit Name	Default	Access	Bit Description
7:0	W_High		R	Channel W High Data Byte
Addr: 0x23		W_Low		
Bit	Bit Name	Default	Access	Bit Description
7:0	W_Low		R	Channel W Low Data Byte

Figure 40:
AS72651 Sensor Calibrated Data Registers (note that the I2C_CAL_SEL register must be set to 0x00 to read these)

Addr: 0x40:0x43		R_Cal		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	R_Cal		R	Channel R Calibrated Data (floating point)
Addr: 0x44:0x47		**S_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	S_Cal		R	Channel S Calibrated Data (floating point)
Addr: 0x48:0x4B		**T_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	T_Cal		R	Channel T Calibrated Data (floating point)
Addr: 0x4C:0x4F		**U_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	U_Cal		R	Channel U Calibrated Data (floating point)
Addr: 0x50:0x53		**V_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	V_Cal		R	Channel V Calibrated Data (floating point)
Addr: 0x54:0x57		**W_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	W_Cal		R	Channel W Calibrated Data (floating point)

Figure 41:
AS72652 Sensor Raw Data Registers

Addr: 0x24		G_High		
Bit	Bit Name	Default	Access	Bit Description
7:0	G_High		R	Channel G High Data Byte
Addr: 0x25		**G_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	G_Low		R	Channel G Low Data Byte
Addr: 0x26		**H_High**		
Bit	Bit Name	Default	Access	Bit Description
7:0	H_High		R	Channel H High Data Byte
Addr: 0x27		**H_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	H_Low		R	Channel H Low Data Byte
Addr: 0x28		**I_High**		
Bit	Bit Name	Default	Access	Bit Description
7:0	I_High		R	Channel I High Data Byte
Addr: 0x29		**I_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	I_Low		R	Channel I Low Data Byte
Addr: 0x2A		**J_High**		
Bit	Bit Name	Default	Access	Bit Description
7:0	J_High		R	Channel J High Data Byte
Addr: 0x2B		**J_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	J_Low		R	Channel J Low Data Byte

Addr: 0x2C		K_High		
Bit	Bit Name	Default	Access	Bit Description
7:0	K_High		R	Channel K High Data Byte
Addr: 0x2D		**K_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	K_Low		R	Channel K Low Data Byte
Addr: 0x2E		**L_High**		
Bit	Bit Name	Default	Access	Bit Description
7:0	L_High		R	Channel L High Data Byte
Addr: 0x2F		**L_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	L_Low		R	Channel L Low Data Byte

Figure 42:
AS72652 Sensor Calibrated Data Registers (note that the I2C_CAL_SEL register must be set to 0x01 to read these)

Addr: 0x40:0x43		G_Cal		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	G_Cal		R	Channel G Calibrated Data (floating point)
Addr: 0x44:0x47		**H_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	H_Cal		R	Channel H Calibrated Data (floating point)
Addr: 0x48:0x4B		**I_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	I_Cal		R	Channel I Calibrated Data (floating point)
Addr: 0x4C:0x4F		**J_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	J_Cal		R	Channel J Calibrated Data (floating point)
Addr: 0x50:0x53		**K_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	K_Cal		R	Channel K Calibrated Data (floating point)
Addr: 0x54:0x57		**L_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	L_Cal		R	Channel L Calibrated Data (floating point)

Figure 43:
AS72653 Sensor Raw Data Registers

Addr: 0x30		A_High		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	A_High		R	Channel A High Data Byte
Addr: 0x31		**A_Low**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	A_Low		R	Channel A Low Data Byte
Addr: 0x32		**B_High**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	B_High		R	Channel B High Data Byte
Addr: 0x33		**B_Low**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	B_Low		R	Channel B Low Data Byte
Addr: 0x34		**C_High**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	C_High		R	Channel C High Data Byte
Addr: 0x35		**C_Low**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	C_Low		R	Channel C Low Data Byte
Addr: 0x36		**D_High**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	D_High		R	Channel D High Data Byte
Addr: 0x37		**D_Low**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	D_Low		R	Channel D Low Data Byte

Addr: 0x38		E_High		
Bit	Bit Name	Default	Access	Bit Description
7:0	E_High		R	Channel E High Data Byte
Addr: 0x39		**E_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	E_Low		R	Channel E Low Data Byte
Addr: 0x3A		**F_High**		
Bit	Bit Name	Default	Access	Bit Description
7:0	F_High		R	Channel F High Data Byte
Addr: 0x3B		**F_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	F_Low		R	Channel F Low Data Byte

Figure 44:
AS72653 Sensor Calibrated Data Registers (note that the I2C_CAL_SEL register must be set to 0x02 to read these)

Addr: 0x40:0x43		A_Cal		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	A_Cal		R	Channel A Calibrated Data (floating point)
Addr: 0x44:0x47		**B_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	B_Cal		R	Channel B Calibrated Data (floating point)
Addr: 0x48:0x4B		**C_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	C_Cal		R	Channel C Calibrated Data (floating point)
Addr: 0x4C:0x4F		**D_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	D_Cal		R	Channel D Calibrated Data (floating point)
Addr: 0x50:0x53		**E_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	E_Cal		R	Channel E Calibrated Data (floating point)
Addr: 0x54:0x57		**F_Cal**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
31:0	F_Cal		R	Channel F Calibrated Data (floating point)

AS72651 I²C Firmware (FW) Update Procedure

- In the FW Update Control register set the Start_XFR bit to 1.
- Write 56K of data to the FW Download register starting with the first byte in the ams file, then proceed the end of the ams 56K file with consecutive writes.
- If desired read the FW Byte Count registers to see which byte is expected to be written next into the FW Download register.
- When the download file is completely written, confirm the action by using the FW Update Control register bit XFR_56K (should =1 if 56K has been downloaded).
- In the FW Update Control register, set the Toggle bit to 1 which will reboot the AS72651 with the new FW after checking the new FW for correct CRC. If the CRC is incorrect the toggle bit will not change and the new FW will not be used.

Figure 45:
Firmware Byte Count High Byte

Addr: 0x60/0xE0		Control_Setup		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Start_XFR	0	R/W	Set to 1 to start firmware update
6	Kill_XFR	0	R/W	Set to 1 to stop firmware update.
5	XFR_56K	0	R	Set to 1 when 56K bytes have been downloaded.
4	Reserved			Reserved, do not use.
3	Toggle	0	R/W	Set to 1 to toggle firmware image partition.
2:0	Reserved			Reserved, do not use.

Figure 46:
Firmware Byte Count, High Byte

Addr: 0x61/0xE1		Firmware Byte Count, High Byte		
Bit	Bit Name	Default	Access	Bit Description
7:0	FWBC_HIGH		R	Firmware byte address to be downloaded next, High Byte

Figure 47:
Firmware Byte Count, Low Byte

Addr: 0x62/0xE2		Firmware Byte Count, Low Byte		
Bit	Bit Name	Default	Access	Bit Description
7:0	FWBC_LOW		R	Firmware byte address to be downloaded next, Low Byte

Figure 48:
Firmware Download

Addr: 0x63/0xE3		Firmware Download		
Bit	Bit Name	Default	Access	Bit Description
7:0	FWLOAD		R/W	Firmware byte to be downloaded

UART Command Interface

If selected by the I2C_ENB pin setting, the UART module implements the TX and RX signals as defined in the RS-232 / V.24 standard communication protocol. Serial flash EPROM is a required operating companion device to enable the UART command interface.

UART Feature List

- Full duplex operation (independent serial receive and transmit registers).
- Factory set to 115.2k Baud
- Supports serial frames with 8 Data Bits, no Parity and 1 Stop Bit.

Operation

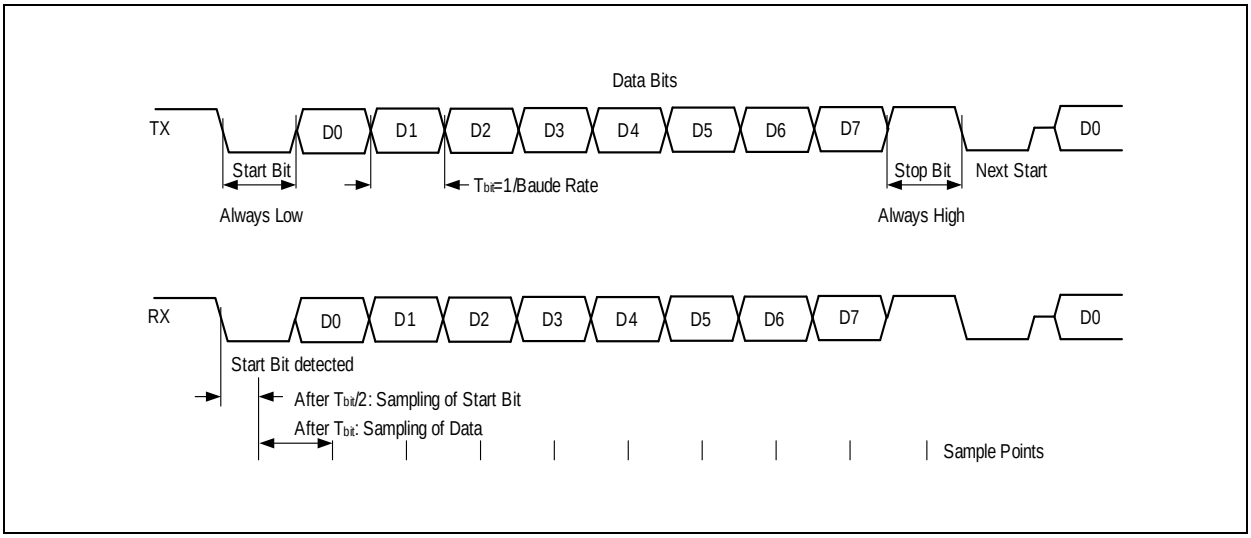
Transmission

If data is available in the transmit FIFO, it will be moved into the output shift register and the data will be transmitted at the configured Baud Rate, starting with a Start Bit (logic zero) and followed by a Stop Bit (logic one).

Reception

At any time, with the receiver being idle, if a falling edge of a start bit is detected on the input, a byte will be received and stored in the receive FIFO. The following Stop Bit will be checked to be logic one.

Figure 49:
UART Protocol



AT Command Interface

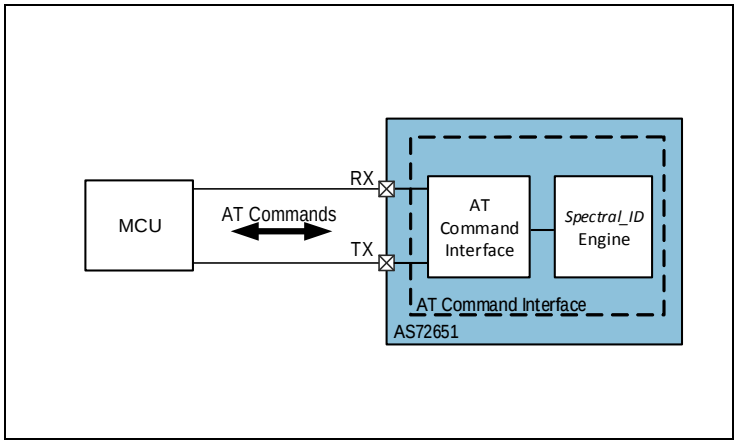
The microprocessor interface to control the AS72651 *Spectral_ID* sensor(s) is via AT Commands across the UART interface. The AS72651 provides a text-based serial command interface borrowed from the “AT Command” model used in early Hayes modems.

For example:

Read DATA value:	ATDATA →	<data>OK
Set the gain of the sensor to 1x:	ATGAIN=0→	OK

The AT Command Interface, shown below provides access to the *Spectral_ID* engine’s control and configuration functions.

Figure 50:
AT Command Interface Block Diagram



In the AT Commands figure below, numeric values may be specified with no leading prefix, in which case they will be interpreted as decimals, or with a leading “0x” to indicate that they are hexadecimal numbers, or with a leading “’b” to indicate that they are binary numbers. The commands are loosely grouped into functional areas. Texts appearing between angle brackets (‘<‘and ‘>‘) are commands or response arguments. A carriage return character, a linefeed character, or both may terminate commands and responses. Note that any command that encounters an error will generate the “ERROR” response shown, for example, in the NOP command at the top of the first table, but has been omitted elsewhere in the interest of readability and clarity.

Note(s): The Figure 51 shows the complete list of all AS7265x AT commands.

Figure 51:
AS7265x AT Commands

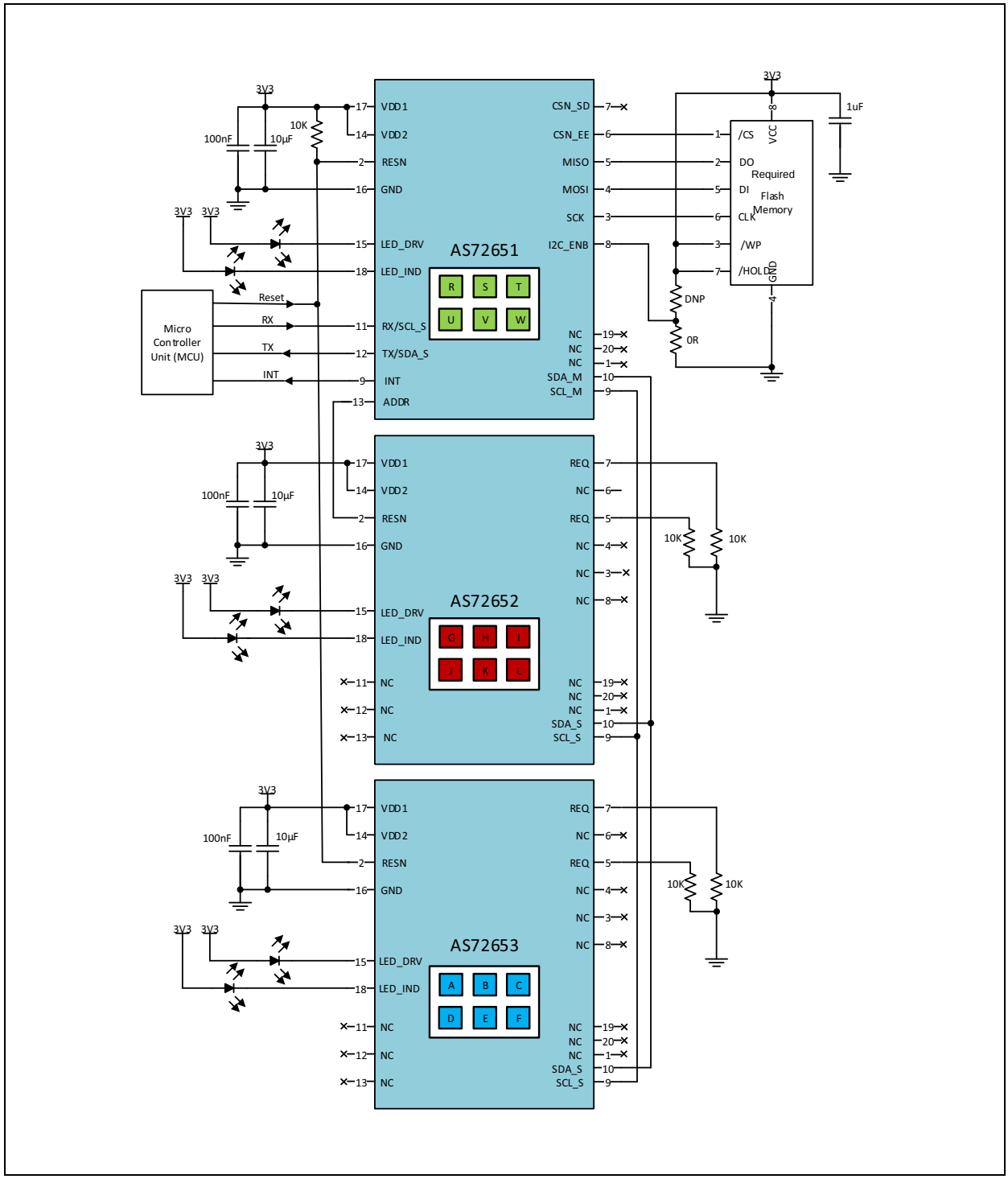
Commands	Response	Description/Parameters
Spectral Data per Channel		
ATCDATA	<R_*value*>, <S_*value*>, <T_*value*>, <U_*value*>, <V_*value*>, <W_*value*>, <J_*value*> , <I_*value*> , <G_*value*> , <H_*value*> , <K_*value*> , <L_*value*> , <D_*value*> , <C_*value*> , <A_*value*> , <B_*value*> , <E_*value*> , <F_*value*> OK	Read calibrated channel in order of device. Read R, S, T, U, V & W data for the AS72651. Returns comma-separated 16 bit floating point values. Read J, I, G, H, K & L data for the AS72652. Returns comma-separated 16 bit floating point values. Returns all zero data if device not present. Read D, C, A, B, E & F data for the AS72653. Returns comma-separated 16 bit floating point values. Returns all zero data if device not present.
Sensor Configuration		
ATINTTIME= <*value*>	OK OK OK	Set integration time for all devices AS72651, AS72652, AS72653. Value should be in the range [1...255], with integration time = <*value*> * 2.8ms. (default value = 255)
ATINTTIME	<*value*> OK <*value*> OK <*value*> OK	Read sensor integration time (same for all devices) integration time = <*value*> * 2.8ms.
ATGAIN= <*value*>	OK OK OK	Set gain for all devices AS72651, AS72652, AS72653: 0=1x, 1=3.7x, 2=16x, 3=64x (default value = 0)
ATGAIN	<*value*>OK <*value*>OK <*value*>OK	Read all gain setting for all devices, returning 0, 1, 2, or 3 as defined immediately above.
ATTEMP	<*value1*><*value2*> <*value3*>OK	Read internal temperature in the order of AS72651, AS72652, AS72653 in celsius
ATTCSMD= <*value*>	OK	Set Sensor Mode 0 = BANK Mode 0; 1 = BANK Mode 1; 2 = BANK Mode 2; (default value = 2)
ATTCSMD	<*value*> OK	Read Sensor Mode, see above

Commands	Response	Description/Parameters
LED Driver Controls		
ATLED0=<*value*>	OK	Sets AS72651 LED_IND: 100=ON, 0=OFF (default value = 0)
ATLED0	<100|0>OK	Reads AS72651 LED_IND setting: 100=ON, 0=OFF
ATLED1=<*value*>	OK	Sets AS72651 LED_DRV: 100=ON, 0=OFF (default value = 0)
ATLED1	<100|0>OK	Reads AS72651 LED_DRV setting: 100=ON, 0=OFF
ATLED2=<*value*>	OK	Sets AS72652 LED_IND: 100=ON, 0=OFF (default value = 0)
ATLED2	<100|0>OK	Reads AS72652 LED_IND setting: 100=ON, 0=OFF
ATLED3=<*value*>	OK	Sets AS72652 LED_DRV: 100=ON, 0=OFF (default value = 0)
ATLED3	<100|0>OK	Reads AS72652 LED_DRV setting: 100=ON, 0=OFF
ATLED4=<*value*>	OK	Sets AS72653 LED_IND: 100=ON, 0=OFF (default value = 0)
ATLED4	<100|0>OK	Reads AS72653 LED_IND setting: 100=ON, 0=OFF
ATLED5=<*value*>	OK	Sets AS72653 LED_DRV: 100=ON, 0=OFF (default value = 0)
ATLED5	<100|0>OK	Reads AS72653 LED_DRV setting: 100=ON, 0=OFF
ATLEDC=<*value*>	OK	Sets LED_IND and LED_DRV current for the AS72651 LED_IND: bits 3:0; LED_DRV: 7:4 bits LED_IND: 'b00=1mA; 'b01=2mA; 'b10=4mA; 'b11=8mA LED_DRV: 'b00=12.5mA; 'b01=25mA; 'b10=50mA; 'b11=100mA (default value = 'b00)
ATLEDC	<value>OK	Reads LED_IND and LED_DRV settings as shown above
ATLEDD=<*value*>	OK	Sets LED_IND and LED_DRV current for the AS72652 LED_IND: bits 3:0; LED_DRV: 7:4 bits LED_IND: 'b00=1mA; 'b01=2mA; 'b10=4mA; 'b11=8mA LED_DRV: 'b00=12.5mA; 'b01=25mA; 'b10=50mA; 'b11=100mA (default value = 'b00)
ATLEDD	<value>OK	Reads the AS72652 LED_IND and LED_DRV settings as shown above
ATLEDE=<*value*>	OK	Sets LED_IND and LED_DRV current for the AS72653 LED_IND: bits 3:0; LED_DRV: 7:4 bits LED_IND: 'b00=1mA; 'b01=2mA; 'b10=4mA; 'b11=8mA LED_DRV: 'b00=12.5mA; 'b01=25mA; 'b10=50mA; 'b11=100mA (default value = 'b00)
ATLEDE	<value>OK	Reads the AS72653 LED_IND and LED_DRV settings as shown above

Commands	Response	Description/Parameters
Miscellaneous System Commands		
AT	OK → Success ERROR → Failure	NOP
ATRST	None	Software Reset – no response
ATVERSW	<*SWversion#*>OK ERROR → Failure	Returns the system software version number
ATVERHW	<*HWversion#*>OK ERROR → Failure	Returns the system hardware revision and product ID, with bits 7:4 containing the part ID, and bits 3:0 yielding the chip revision value.
ATPRES	<value>OK	0 Only AS72651 present 1 AS72651,AS72652 present 2 AS72651,AS72653 present 3 AS72651,AS72652 and AS72653 present
ATINTRP=<*value*>	OK	Enables AS72651 interrupt operation; 1=ON, 0=OFF
ATINTRP	<100|0>OK	Reads AS72651 Interrupt mode; 1=ON, 0=OFF
Firmware Update		
ATFWU=<*value*>	OK	<*value*>= 16-bit checksum. Initializes the firmware update process. Number of bytes that follow are always 56k bytes
ATFW=<*value*>	OK	Download new firmware Up to 7 bytes represented as hex chars with no leading or trailing 0x. Repeat command till all 56k bytes of firmware are downloaded
ATFWA	OK	Causes target address for FW updates to advance. Should be called after every successful "OK" returned after "ATFW=<*value*>" command usage.
ATFWS	OK	Causes the active image to switch between the two possible current images and then resets the IC

Application Information

Figure 52:
Typical AS7265x 18-Channel Application Circuit

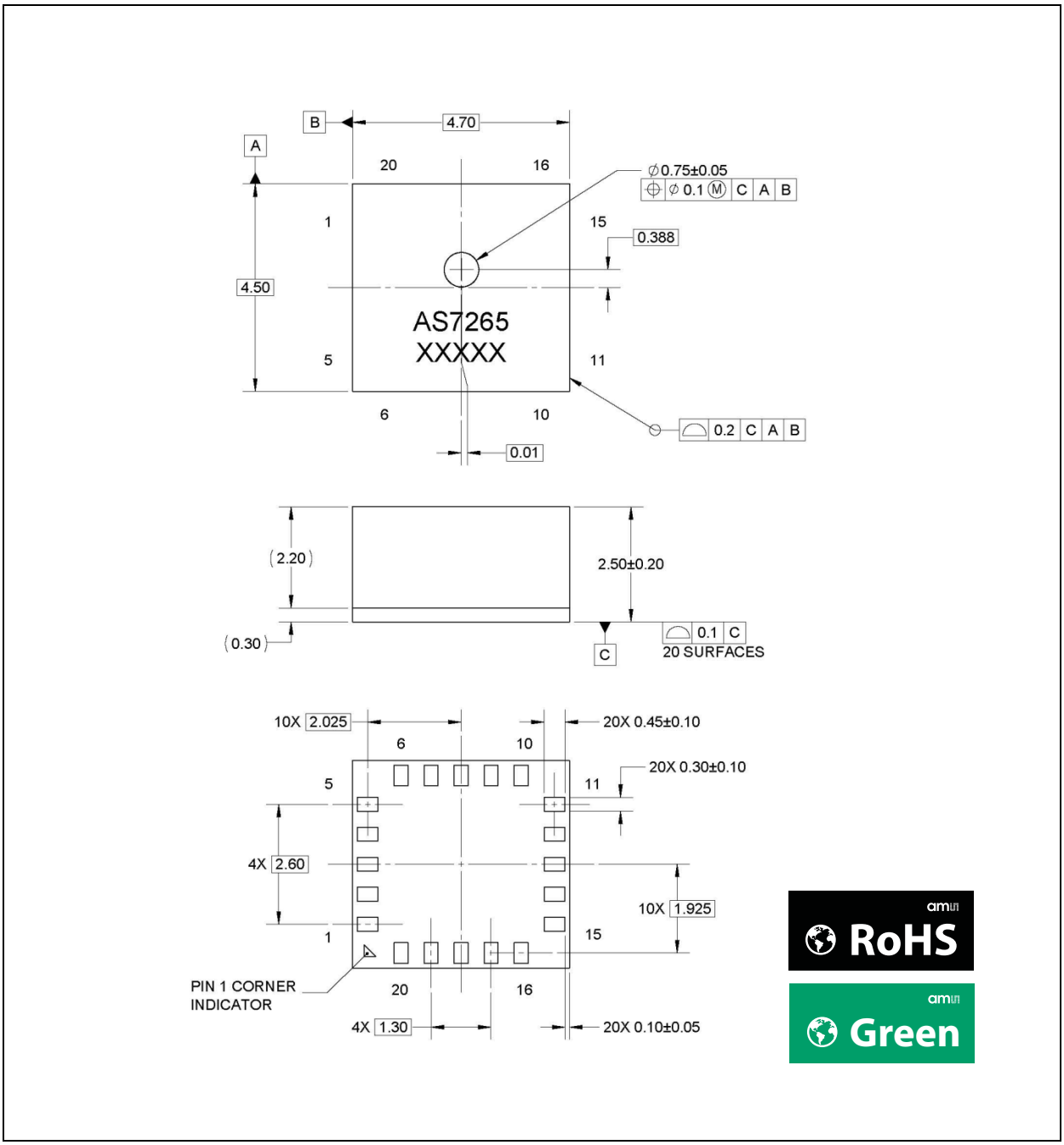


Note(s):

1. For each AS7265x device, orientation of the device aperture to any light source(s) will determine spectral content to be measured. For example with the proper orientation, sensors on the AS72651 can be used to measure light from the LEDs on the AS72652 and/or AS76253.
2. The AS72651 is required while the AS72652 and AS72653 are both optional for a total solution of 6, 12 or 18 channels.

Package Drawings & Markings

Figure 53:
Package Drawing



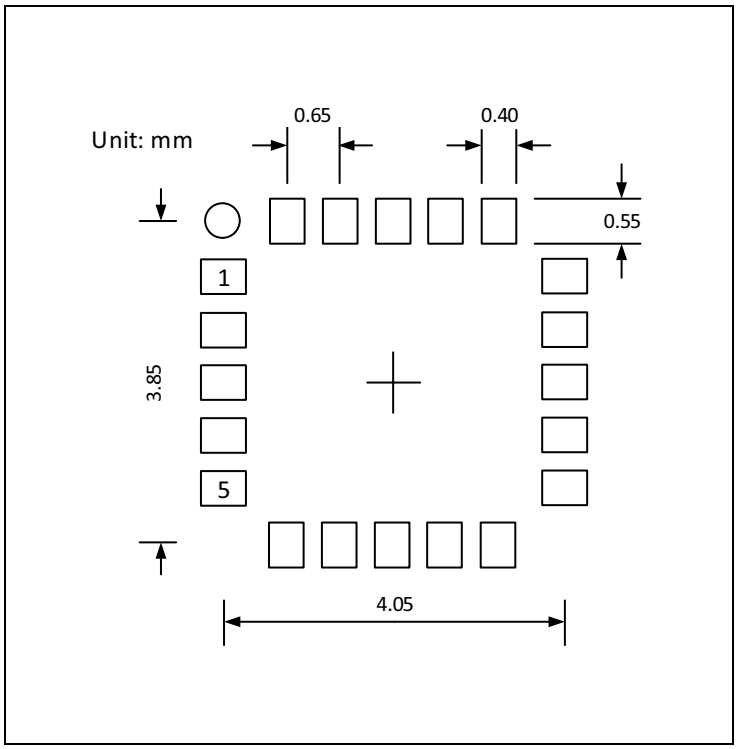
Note(s):

1. All dimensions are in millimeters.
2. XXXXX = tracecode.
3. Unless otherwise specified tolerances are: Angular (±.5°), Two Place Decimal (±.1), Three Place Decimal (±.05).
4. Contact finish is Au.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

PCB Pad Layout

Suggested PCB pad layout guidelines for the LGA device are shown. Flash Gold is recommended as a surface finish for the landing pads.

Figure 54:
Recommended PCB Pad Layout (Top View)

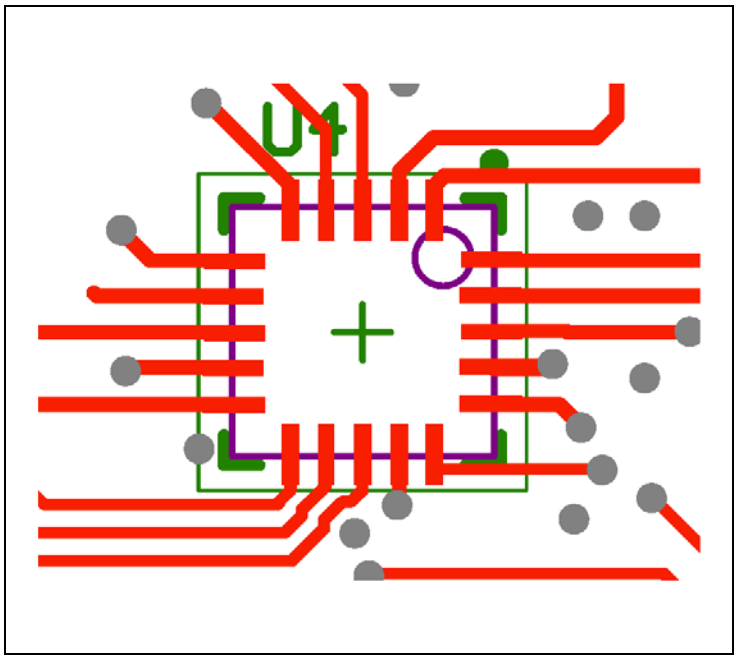


Note(s):

1. Unless otherwise specified, all dimensions are in millimeters.
2. Add 0.05mm all around the nominal lead width and length for the PCB pad land pattern.
3. This drawing is subject to change without notice.

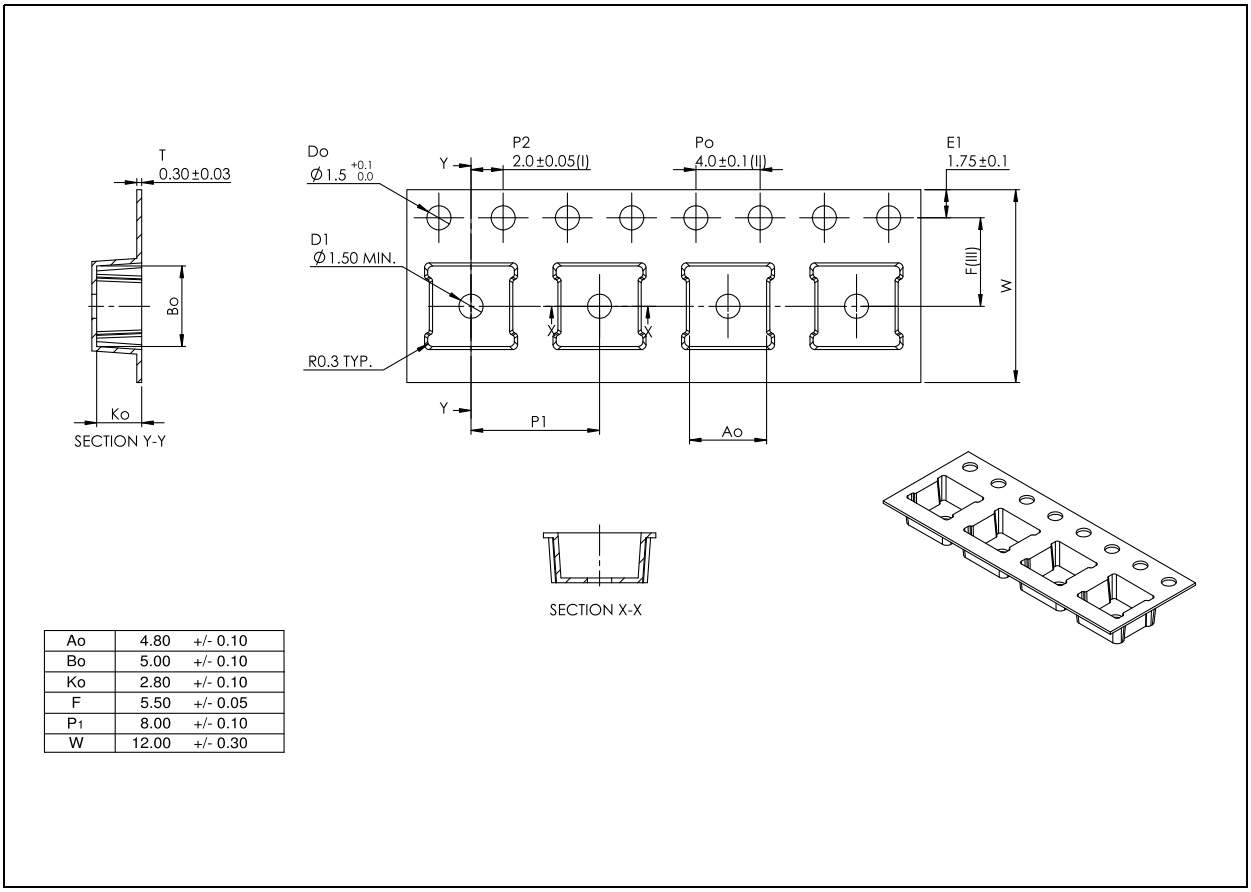
In order to prevent interference, avoid trace routing feedthroughs with exposure directly under the AS7265x devices. An example routing is illustrated in the Figure 55.

Figure 55:
Typical Layout Routing



Mechanical Data

Figure 56:
Tape & Reel Information



Ao	4.80	+/- 0.10
Bo	5.00	+/- 0.10
Ko	2.80	+/- 0.10
F	5.50	+/- 0.05
P_1	8.00	+/- 0.10
W	12.00	+/- 0.30

Note(s):

1. All dimensions in millimeters unless of otherwise stated.
2. Measured from centreline of sprocket hole to centreline of pocket.
3. Cumulative tolerance of 10 sprocket holes is ±0.20.
4. Measured from centreline of sprocket hole to centreline of pocket.
5. Other material available.

Soldering & Storage Information

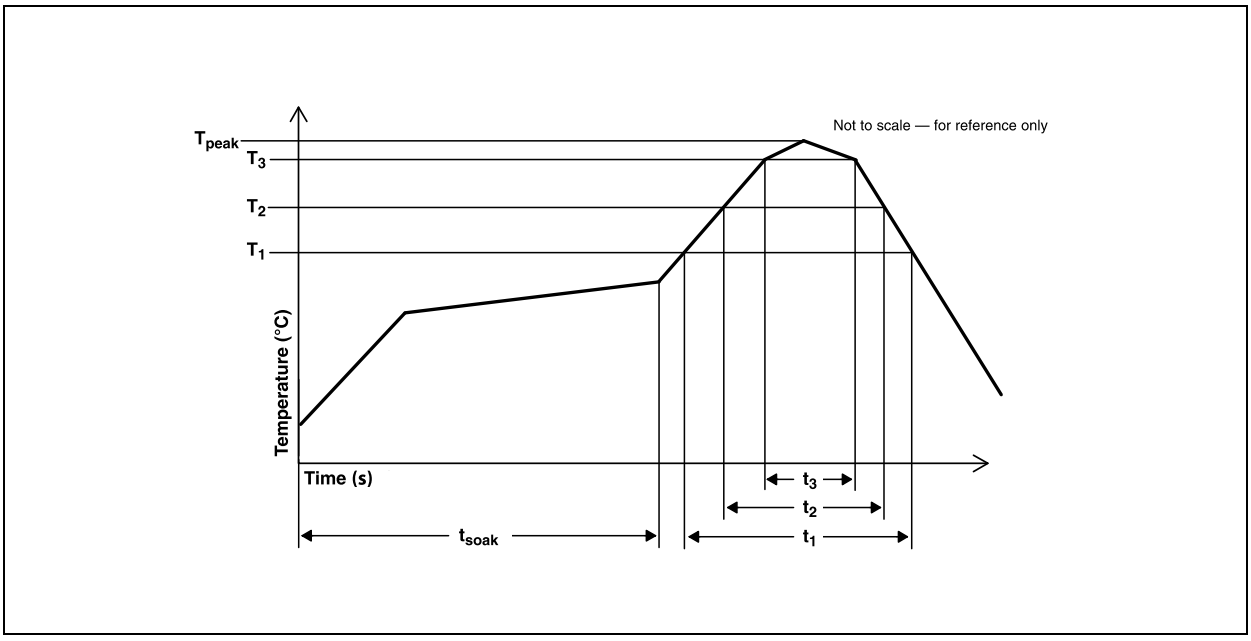
Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 57:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5°C/s
Soak time	t_{SOAK}	2 to 3 minutes
Time above 217°C(T_1)	t_1	Max 60s
Time above 230°C(T_2)	t_2	Max 50s
Time above T_{peak} - 10°C(T_3)	t_3	Max 10s
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max -5°C/s

Figure 58:
Solder Reflow Profile Graph



Manufacturing Process Considerations

The AS72651 package is compatible with standard reflow no-clean and cleaning processes including aqueous, solvent or ultrasonic techniques. However, as an open-aperture device, precautions must be taken to avoid particulate or solvent contamination as a result of any manufacturing processes, including pick and place, reflow, cleaning, integration assembly and/or testing. Temporary covering of the aperture is allowed. To avoid degradation of accuracy or performance in the end product, care should be taken that any temporary covering and associated sealants/debris are thoroughly removed prior to any optical testing or final packaging.

Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping.

Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

Floor Life: 168 hours

Ambient Temperature: <30°C

Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 59:
Ordering Information

Ordering Code	Package	Marking	Description	Delivery Form	Delivery Quantity
AS72651-BLGT	20-pin LGA	AS7265	Smart 6-Channel NIR Spectral_ID Sensor with Electronic Shutter and 18-Channel AS7265x Master Capability	Tape & Reel	2000 pcs/reel
AS72652-BLGT	20-pin LGA	AS7266	Smart 6-Channel NIR Spectral_ID Sensor with Electronic Shutter	Tape & Reel	2000 pcs/reel
AS72653-BLGT	20-pin LGA	AS7267	Smart 6-Channel Spectral_ID Sensor with Electronic Shutter	Tape & Reel	2000 pcs/reel

Note(s):

1. The AS72651 is required for operation of either the AS72652 or AS72653.
2. A required companion serial flash memory is required for functionality and should be ordered from the flash memory supplier or their authorized channels. Selected device types must be ams verified and at the time of writing include Adesto Technologies AT25SF041-SSHD-B, or Macronix MX25L4006EM1I-12G. Visit the **ams** download page for your AS72xx device at download.ams.com and consult current firmware release notes for currently supported devices. More details and alternative flash memories please see the User Guide for Flash Updating.
3. AS72651 flash memory software is available from **ams**.

Buy our products or get free samples online at:
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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 1-02 (2017-Jun-12) to current revision 1-03 (2017-Oct-17)	Page
Updated text under AS7265x 18 Channel Spectral_ID Detector Overview	17
Added Required Flash Memory section	21
Updated text under UART Command Interface	47
Added note above Figure 51	48
Updated Figure 51	49
Updated Figure 52	52
Updated notes under Figure 59	60

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide