



Application Note: AS505x – Disabling low power mode

AS505x

Disabling lower power mode

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Revision History

Revision	Date	Owner	Description
0.9	27.11.2013	mzie	Initial version
1.0	03.12.2013	rei	Approved

1 General Description

This application note describes how to disable the low power mode function of the AS5050 and AS5055 magnetic position sensors.

To reduce power consumption the AS5050/AS5055 offers low power features. The IC enters a sleep mode when no commands or calculations are executed. To exit the sleep mode a READ ANGLE command via the SPI interface has to be sent.

Some applications require faster readout intervals from the IC. Therefore you have the possibility to disable the low power mode and enter a continuous mode. As a drawback the power consumption will increase. In figure 1 you can see the System Parameters for the power consumption.

Figure 1: System Parameters for power consumption

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{ON}	Current consumption	Max. readout rate			8.5	mA
I_{OFF1}	Current consumption	Activated POR (default)			33	μ A
I_{OFF2}	Current consumption	Deactivated POR			3	μ A

With low power mode activated the power consumption of the AS5050/AS5055 depends on the interval, at which the microcontroller reads an angle over the SPI interface and can be calculated with the formula shown below.

$$I_{avg} = \frac{t_{on} * I_{on} + t_{off} * I_{off}}{t_{on} + t_{off}}$$

t_{ON}	=	On-Time for power-up and angle measurement	520 μ s
t_{OFF}	=	Pause interval between measurements	
I_{ON}	=	Current consumption in active mode	8.5 mA
I_{OFF}	=	Current consumption in sleep mode	33 μ A

2 Disabling the low power mode

With deactivated low power mode a maximum power consumption of 8.5 mA can be assumed. To disable the lower power mode the bit **pd_disable** in the **Test Control Register 1** has to be set. Figure 2 shows the Test Control Register 1.

Figure 2: Test Control Register 1 (0x3FC0)

Register	Bit	R/W	Description
pd_disable	0	R/W	Disables the low power mode
ext_clk_en	1	R/W	Enables the external clock pin
sel_otp	2	R/W	Enables PPTRIM functionality
scan_tst_en	3	R/W	Enables scan functionality
wire mode	4	R	

Figure 3 shows a WRITE command to the Test Control Register 1 with address (0x3FC0).

Figure 3: WRITE command to Test Control Register 1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R/W	Address <14:1>														PAR
	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1
	0x3FC0															

Figure 4: WRITE DATA command to Test Control Register 1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data <15:2>														DC	PAR
	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Note: When sending a SOFTWARE RESET, MASTER RESET command or doing Power-On Reset to the AS5050/AS5055 the default values are loaded from the OTP. To disable the lower power mode permanently a programming of the OTP registers has to be done.

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