Application Note: AS3933-AN02 – Demodulator/Data Slicer

AS3933

Demodulator/Data Slicer

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Revision History

Revision	Date	Owner	Description
1.0	15.10.2012	JRY	Description Data Slicer

1 General Description

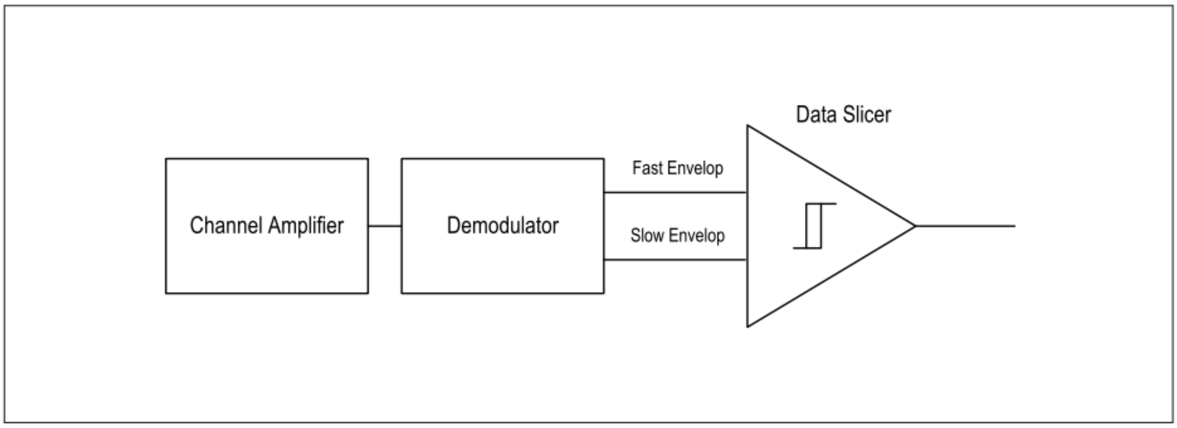
This application note describes the demodulator and data slicer blocks of the AS3933 and how to set them up. Specifically, the dynamic threshold and absolute threshold will be looked at in more detail.

2 Demodulator/Data Slicer

After the channel selector decides on the channel amplifier with highest RSSI, it connects that channel to the demodulator. The demodulator returns the signal to base-band and, furthermore, extracts two signals. The first one is a fast envelope of the base-band signal, which will be used to recover the digital information. The second signal is a slow envelope of the incoming bit stream, i.e. the time constant of the circuit is bigger than the time constant of the circuit for the fast envelope. The slow envelope therefore represents an average value of the incoming bit stream. Those two signals are then fed to the data slicer. There the two signals are compared, with the slow envelope used as trigger threshold. A block diagram of this circuit is shown in figure 1.

Figure 1:

Concept Block Diagram of the Demodulator and Data Slicer

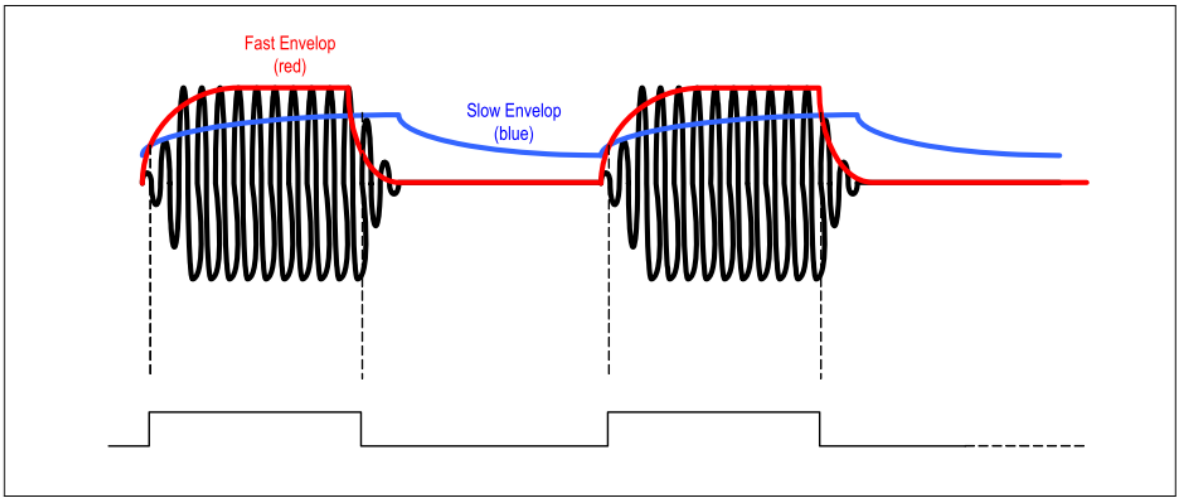


3 Demodulator

The output of the demodulator consists of two signals. A representation of the input signal and the output of the demodulator are illustrated in figure 2.

Figure 2:

Fast and Slow Envelope Signals



3.1 Fast Envelope Time Constant

The time constants of the demodulator need to be adjusted according to the bit rate and preamble length to optimize its performance. If the bit rate increases, the time constant for the fast envelope needs to decrease. The time constant for the fast envelope can be set in register R3<2:0>. The recommended settings for different data rates, as they are given in the data sheet on page 26, can be seen in figure 3. For smaller time constants the higher noise that is injected needs to be considered.

Figure 3:

Bit Setup of the Fast Envelope's Time Constant for Different Symbol Rates

R3<2>	R3<1>	R3<0>	Symbol Rate [Manchester symbol/s]
0	0	0	4096
0	0	1	2184
0	1	0	1490
0	1	1	1130
1	0	0	910
1	0	1	762
1	1	0	655
1	1	1	512

3.2 Slow Envelope Time Constant

The slow envelope can be optimized to improve the noise immunity of the data slicer. The deciding factor here is the preamble length. Increasing the noise immunity of the data slicer, which is equivalent to increasing the slow envelope's time constant in case the dynamic threshold is used, means that the preamble has to be made longer. The correlation between the slow envelope's time constant and the minimum preamble length is given in figure 4. The times for the preamble length are minimum required values. It is recommended to prolong the preamble. These values are taken from table 21 in the data sheet.

Figure 4:

Minimum Preamble Length for Different Slow Envelope Time Constants

R3<5>	R3<4>	R3<3>	Minimum Preamble Length [ms]
0	0	0	0.8
0	0	1	1.15
0	1	0	1.55
0	1	1	1.9
1	0	0	2.3
1	0	1	2.65
1	1	0	3
1	1	1	3.5

The preamble is a series of alternating zeros and ones which separates the data from the carrier burst. Prolonging the preamble gives the slow envelope more time to settle at a center voltage value before the data bits come in.

4 Data Slicer

4.1 Dynamic Threshold

The outputs of the demodulator, the fast and slow envelopes, are further processed by the data slicer. The data slicer uses the voltage level of the slow envelope as trigger level. Each time the fast envelope signal crosses the slow envelope, the comparator triggers. With register R3<7:6> the comparator's hysteresis can be controlled. The settings are shown in figure 5.

Figure 5:

Comparator Hysteresis Settings

R3<7>	R3<6>	Hysteresis Setting
0	0	40mV, both edges
0	1	40mV, only positive edges
1	0	20mV, both edges
1	1	20mV, only positive edges

The bit pattern that is created in this way will then represent the desired signal. The output of the data slicer in relation to its input is shown in figure 2.

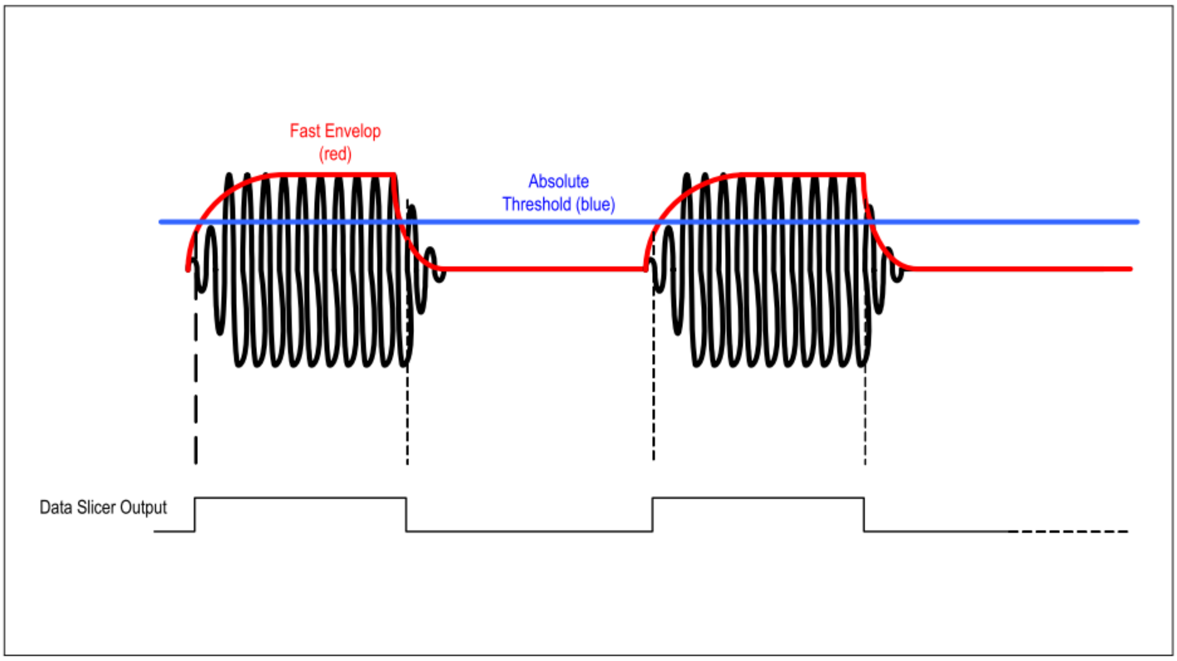
4.2 Absolute Threshold

In case the incoming signal has a duty cycle far away from 50%, the slow envelope will not work very well as trigger level. The slow envelope represents an average value of the demodulated signal. If the duty cycle is too far away from 50%, the slow envelope's voltage level will be either too high or too low, but not in the center of the signal range where it is supposed to be. Therefore, an absolute threshold for the data slicer can be enabled with bit R1<7>. Setting this bit 'high' will automatically deactivate the dynamic threshold. Respectively, the bits in register R3<5:3>, which control the preamble length, will no longer influence the data slicer's noise immunity. The preamble length can be therefore set to its minimum value.

The voltage level of the absolute threshold is set to the middle of the demodulator's output dynamic range. The absolute threshold level can be reduced by setting bit R2<7> to 'high' in case the environment is not noisy.

Figure 6:

Data Slicer Input and Output with an Absolute Threshold



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