



Application Note: AS3722– OTP Specification -11

AS3722-BCTT-11

AS3722-BWLT-11

OTP Specification -11

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Revision History

Revision	Date	Owner	Description
0.90	19.3.2014	pkm	Initial version
0.91	21.3.2014	pkm	typo correction
1.00	28.3.2014	pkm	added NVPN and MPN

1 General Description

The “-11” OTP version is applicable for the following ordering codes:

Ordering code	MPN	Reel Size	NVPN
AS3722-BCTT-11	193600022	500pcs	315-0312-000

The silicon version used for these build used 1v21.

2 OTP Description

File name: AS3722_OTP-11_nVidia_1V35mem_3S_-200mV_SD3_20140317.txt

2.1 GUI SW screenshot

Timeslot 0		
SD3 <input type="text"/>	3.3000V <input type="text"/>	<input checked="" type="radio"/> 3MHz
<input checked="" type="checkbox"/> Delayed		<input type="radio"/> 4MHz
Timeslot 1		
LDO3 <input type="text"/>	1.1000V <input type="text"/>	Mode <input type="text"/> PMOS LDO tracking <input type="text"/>
<input checked="" type="checkbox"/> Delayed		
Timeslot 2		
SD1 <input type="text"/>	1.1000V <input type="text"/>	<input checked="" type="radio"/> Normal
<input checked="" type="checkbox"/> Delayed		<input type="radio"/> Low Power
Timeslot 3		
Not Used <input type="text"/>		
<input checked="" type="checkbox"/> Delayed		
Timeslot 4		
Not Used <input type="text"/>		
<input checked="" type="checkbox"/> Delayed		
Timeslot 5		
Not Used <input type="text"/>		
<input checked="" type="checkbox"/> Delayed		
Timeslot 6		
Not Used <input type="text"/>		
<input checked="" type="checkbox"/> Delayed		
Timeslot 7		
SD5 <input type="text"/>	1.8000V <input type="text"/>	<input checked="" type="radio"/> 3MHz
<input checked="" type="checkbox"/> Delayed		<input type="radio"/> 4MHz

Timeslot 8	
GPIO2 <input type="checkbox"/> Delayed	<input checked="" type="checkbox"/> invert IO Normal I/O operation mode Output (Push/pull) VDDL_GPIO
Timeslot 9	
SD2 <input checked="" type="checkbox"/> Delayed	1.3500V <input type="radio"/> 3MHz <input type="radio"/> 4MHz
Timeslot 10	
LD00 <input checked="" type="checkbox"/> Delayed	1.0500V <input type="radio"/> 150mA <input checked="" type="radio"/> 300mA
Timeslot 11	
GPIO1 <input checked="" type="checkbox"/> Delayed	<input checked="" type="checkbox"/> invert IO Normal I/O operation mode Output (Push/pull) VDDL_GPIO
Timeslot 12	
GPIO4 <input type="checkbox"/> Delayed	<input type="checkbox"/> invert IO Normal I/O operation mode Output (Push/pull) VDDL_GPIO
Timeslot 13	
Not Used <input type="checkbox"/> Delayed	
Timeslot 14	
Not Used <input type="checkbox"/> Delayed	
Timeslot 15	
Not Used <input type="checkbox"/> Delayed	

2.2 Start-up file

Fuse Register Settings

- Register 0xa7 = 0x18 (00011000b)
- Register 0xa8 = 0x4f (01001111b)
- Register 0xa9 = 0xe4 (11100100b)
- Register 0xaa = 0x57 (01010111b)
- Register 0xab = 0x7e (01111110b)
- Register 0xac = 0x41 (01000001b)
- Register 0xad = 0x00 (00000000b)
- Register 0xae = 0x00 (00000000b)
- Register 0xaf = 0x12 (00010010b)
- Register 0xb0 = 0xee (11101110b)

Register 0xb1 = 0x33 (00110011b)
Register 0xb2 = 0x7e (01111110b)
Register 0xb3 = 0x59 (01011001b)
Register 0xb4 = 0xc1 (11000001b)
Register 0xb5 = 0x32 (00110010b)
Register 0xb6 = 0x00 (00000000b)
Register 0xb7 = 0xbf (10111111b)
Register 0xb8 = 0xcc (11001100b)
Register 0xb9 = 0x00 (00000000b)
Register 0xba = 0x00 (00000000b)
Register 0xbb = 0x5c (01011100b)
Register 0xbc = 0x00 (00000000b)
Register 0xbd = 0x50 (01010000b)
Register 0xbe = 0xb8 (10111000b)
Register 0xbf = 0x2a (00101010b)
Register 0xc0 = 0x87 (10000111b)
Register 0xc1 = 0x3c (00111100b)
Register 0xc2 = 0x90 (10010000b)
Register 0xc3 = 0x8a (10001010b)
Register 0xc4 = 0x87 (10000111b)
Register 0xc5 = 0x54 (01010100b)
Register 0xc6 = 0xcc (11001100b)
Register 0xc7 = 0x07 (00000111b)
Register 0xc8 = 0x00 (00000000b)
Register 0xc9 = 0xcc (11001100b)
Register 0xca = 0x00 (00000000b)
Register 0xcb = 0x00 (00000000b)
Register 0xcc = 0x05 (00000101b)
Register 0xcd = 0xcc (11001100b)
Register 0xce = 0x00 (00000000b)
Register 0xcf = 0x00 (00000000b)