

Product Document



Application Note: AS3722– OTP Specification -10

AS3722-BCTT-10

AS3722-BWLT-10

OTP Specification -10

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Revision History

Revision	Date	Owner	Description
0.90	26.11.2013	pkm	Initial version
1.00	28.11.2013	pkm	Added NVPN
1.09	17.1.2014	pkm	Updates for chip version 1v21
1.10	23.1.2014	pkm	Added NVPN
1.20	28.3.2014	pkm	added MPN

1 General Description

The “-10” OTP version is applicable for the following ordering codes:

Ordering code	MPN	Reel Size	NVPN
AS3722-BCTT-10	193600018	500pcs	315-0282-000

The silicon version used for these build used 1v21.

2 OTP Description

File name: AS3722_OTP-10_nVidia_1V35mem_2S_-200mV_em_shutdownN_20131125.txt

2.1 GUI SW screenshot

General Settings

UID Reset Slots

Delay Interval: 4 ms

Reset time: 11ms ncells:

Reset Voltage Rise: 5.9V 2 cell: reset_rise = 2*(2.5...3.6) = 5.0...7.2

vsup_min: 4.5V

SupResEn auto off

em_shutdown_direct pwr_off vsuplow

rtc_on wtdg_on Watchdog mode: INT only

ENABLE2_invert ENABLE3_invert GPIO12 pulldown

LID_pwr_on LID invert GPIO12 input

ac_ok_pwr_on ac_ok_invert therm_invert

onkey_lpress_res onkey_invert I2C pullup

Onkey Shutdown Delay: 8sec

SD2 fast SD2 hi_curr SD0 -200mV offset

SD3 fast SD3 slave

SD4 fast SD4 slave multiphase clock: 1.35 MHz

SD5 fast SD5 slave LDO3 offset: no offset

sd0_vmax: Protection disabled sd0_trim_gm: fast

sd6_vmax: Protection disabled sd1_trim_gm: fast

sd6_trim_gm: fast

Timeslot 0			
LDO3	1.1000V	Mode	PMOS LDO tracking
<input checked="" type="checkbox"/> Delayed			
Timeslot 1			
SD1	1.1000V	<input checked="" type="radio"/> Normal	<input type="radio"/> Low Power
<input checked="" type="checkbox"/> Delayed			
Timeslot 2			
Not Used			
<input checked="" type="checkbox"/> Delayed			
Timeslot 3			
Not Used			
<input checked="" type="checkbox"/> Delayed			
Timeslot 4			
Not Used			
<input checked="" type="checkbox"/> Delayed			
Timeslot 5			
Not Used			
<input checked="" type="checkbox"/> Delayed			
Timeslot 6			
SD5	1.8000V	<input checked="" type="radio"/> 3MHz	<input type="radio"/> 4MHz
<input checked="" type="checkbox"/> Delayed			
Timeslot 7			
GPIO2	<input checked="" type="checkbox"/> invert	IO	Normal I/O operation
<input type="checkbox"/> Delayed		mode	Output (Push/pull) VDDL_GPIO

Timeslot 8	
SD2	1.3500V <input checked="" type="radio"/> 3MHz <input type="radio"/> 4MHz
<input checked="" type="checkbox"/> Delayed	
Timeslot 9	
LDO0	1.0500V <input type="radio"/> 150mA <input checked="" type="radio"/> 300mA
<input checked="" type="checkbox"/> Delayed	
Timeslot 10	
GPIO1	<input checked="" type="checkbox"/> invert ID Normal I/O operation mode Output (Push/pull) VDDL_GPIO
<input checked="" type="checkbox"/> Delayed	
Timeslot 11	
GPIO4	<input type="checkbox"/> invert ID Normal I/O operation mode Output (Push/pull) VDDL_GPIO
<input type="checkbox"/> Delayed	
Timeslot 12	
Not Used	
<input type="checkbox"/> Delayed	
Timeslot 13	
Not Used	
<input type="checkbox"/> Delayed	
Timeslot 14	
Not Used	
<input type="checkbox"/> Delayed	
Timeslot 15	
Not Used	
<input type="checkbox"/> Delayed	
Timeslot 16	
Not Used	

2.2 Start-up file

Fuse Register Settings

Register 0xa7 = 0x38 (00111000b)
 Register 0xa8 = 0x4f (01001111b)
 Register 0xa9 = 0xa4 (10100100b)
 Register 0xaa = 0x57 (01010111b)
 Register 0xab = 0x7e (01111110b)
 Register 0xac = 0x41 (01000001b)
 Register 0xad = 0x00 (00000000b)
 Register 0xae = 0x00 (00000000b)

Register 0xaf = 0x11 (00010001b)
Register 0xb0 = 0xfb (11111011b)
Register 0xb1 = 0x13 (00010011b)
Register 0xb2 = 0x59 (01011001b)
Register 0xb3 = 0x32 (00110010b)
Register 0xb4 = 0xcc (11001100b)
Register 0xb5 = 0x00 (00000000b)
Register 0xb6 = 0x00 (00000000b)
Register 0xb7 = 0x2f (00101111b)
Register 0xb8 = 0xcc (11001100b)
Register 0xb9 = 0x00 (00000000b)
Register 0xba = 0x00 (00000000b)
Register 0xbb = 0xa5 (10100101b)
Register 0xbc = 0x50 (01010000b)
Register 0xbd = 0x87 (10000111b)
Register 0xbe = 0x2e (00101110b)
Register 0xbf = 0x02 (00000010b)
Register 0xc0 = 0x3c (00111100b)
Register 0xc1 = 0x8a (10001010b)
Register 0xc2 = 0xc9 (11001001b)
Register 0xc3 = 0x87 (10000111b)
Register 0xc4 = 0x07 (00000111b)
Register 0xc5 = 0x55 (01010101b)
Register 0xc6 = 0xcc (11001100b)
Register 0xc7 = 0x00 (00000000b)
Register 0xc8 = 0x00 (00000000b)
Register 0xc9 = 0xcc (11001100b)
Register 0xca = 0x00 (00000000b)
Register 0xcb = 0x00 (00000000b)
Register 0xcc = 0x05 (00010101b)
Register 0xcd = 0xcc (11001100b)
Register 0xce = 0x00 (00000000b)
Register 0xcf = 0x00 (00000000b)