Product Document

Published by
ams OSRAM Group

Application Note

AS3701A-BWLM-52

OTP specification for AS3701A-BWLM-52

Content Guide

1 General Description

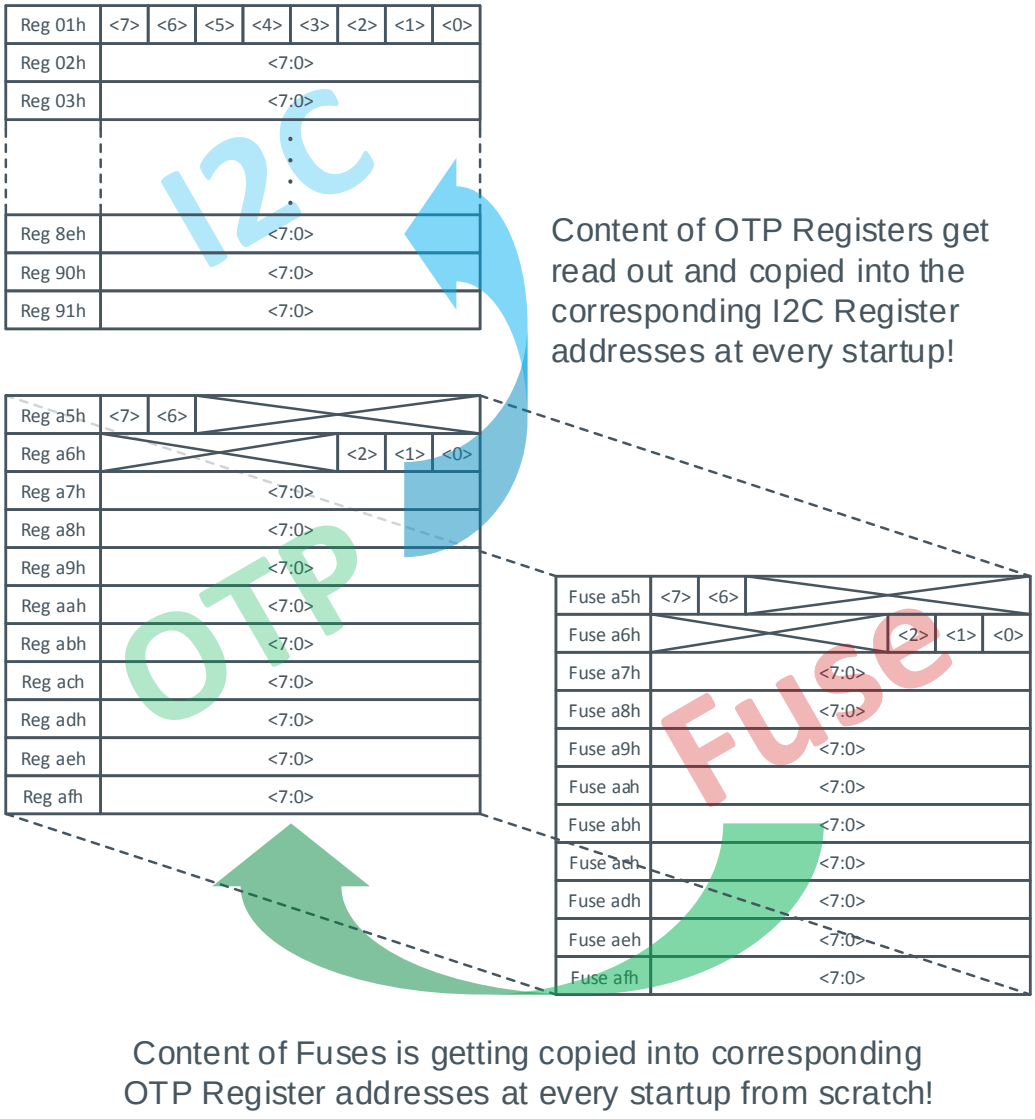
This Application Note describes the OTP settings of the AS3701A-BWLM-52 variant.

The AS3701 has a One Time Programmable (OTP) Boot ROM, which is factory pre-programmed at final test and leads to a defined default startup behavior of AS3701.

2 Detailed Description of the OTP registers functionality

2.1 General Register Block Description

Figure 1: Overview of the OTP registers functionality



2.1.1 I2C Register

- Accessible via I2C every time (READ/WRITE)
- Content get lost when the system power (VSUP) fails
- Reset to their default state, when a reset command gets initiated

2.1.2 OTP Registers

- Only READ via I2C possible
- Entering testmode is mandatory to WRITE onto this registers
- Trimming of chip and setting of dedicated startup sequence
- Bit setting information comes from Fuse block
- Content get lost when the system power (VSUP) fails

2.1.3 OTP Fuses

- Contain all trimming and startup sequence settings
- OTP fuse burning routine:
    - Entering Testmode
    - WRITE correct bit setting into OTP Registers
    - BURN this information to the corresponding OTP fuses
- Programmed fuses will never lose their information
- Bit setting is getting copied anytime into OTP registers, when a startup from scratch occurs (POR level)

2.2 Startup from scratch

Whenever AS3701 has a startup from scratch (first battery insertion or charger adapter insertion without battery) and VSUP increases the POR voltage, the content of the ROM fuses will get read out and copied directly into the corresponding OTP register addresses (see the green arrow)!

If the VSUP voltage further increases and reaches the Reset Voltage Rise level, the content of the OTP registers will get read out and copied directly into the corresponding register addresses (see the blue arrow)!

2.3 Startup during normal operation

During normal operation, a startup will be initiated whenever the AS3701 gets

- a reset command or
- a wake-up command from stand-by mode or
- a wake-up command from power-off mode

A startup during normal operation implies, that the AS3701 is always supplied via a battery or a charger adapter and the VSUP is always higher than the Reset Voltage Rise level. In this case, at every startup only the content of the OTP registers will be copied into the corresponding register addresses.

If the VSUP level would fall below the POR level, all registers (I2C & OTP registers) will loose their content and consequently the following startup would be from scratch containing the OTP settings stored in the fuses!

3 Detailed Explanation of the AS3701A-BWLM-52 OTP settings

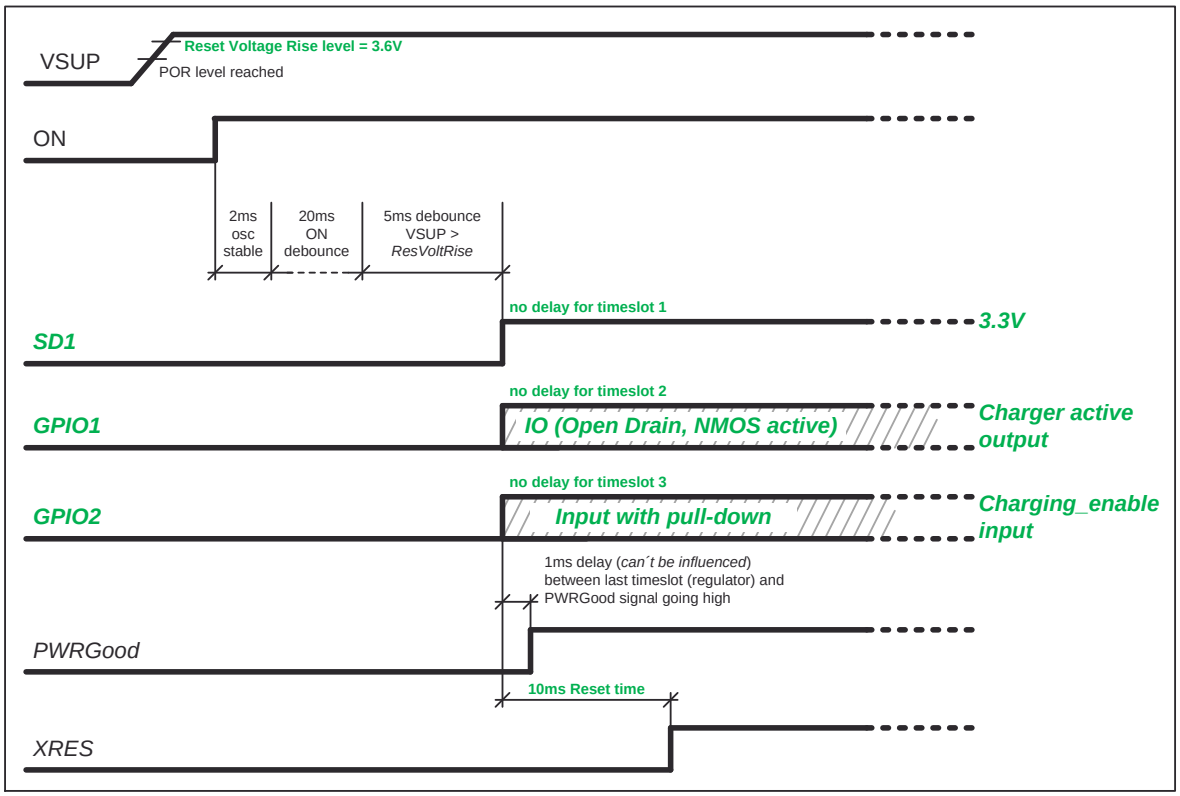
In this chapter, each OTP setting of the AS3701A-BWLM-52 variant will be explained in detail.

3.1 Timeslots

The following diagram should illustrate the startup behavior of the regulators, which are part of the OTP setting!

All the green marked parameters are OTP defined settings!

Figure 2: Startup digram for AS3701A-BWLM-52



For the AS3701A-BWLM-52 variant, there´re 3 timeslots used.

- Timeslot 1 contains the configuration of SD1. The output voltage of SD1 is set to 3.3V and the switching frequency is set to 2MHz!
  The configuration of timeslot 1 with SD1 is done with the bits <3:0> of fuse register aah.
  The parameter settings of SD1 is done with the bits <7:0> of fuse register abh.
- Timeslot 2 contains the configuration of GPIO1. The mode of GPIO1 is set to IO (open drain, NMOS active), the GPIO1 special function is defined as Charger active output and it´s configured as active low (inverted)!
  The configuration of timeslot 2 with GPIO1 is done with the bits <7:4> of fuse register aah.
  The parameter settings of GPIO1 is done with the bits <7:0> of fuse register ach.
- Timeslot 3 contains the configuration of GPIO2. The mode of GPIO2 is set to Input with pull-down, the GPIO2 special function is defined as Charger enable input and it´s configured as active low (inverted)!
  The configuration of timeslot 3 with GPIO2 is done with the bits <3:0> of fuse register adh.
  The parameter settings of GPIO2 is done with the bits <7:0> of fuse register aeh.

3.2 Delay Interval

The delay interval, which defines the delay of a timeslot referring to it´s previous timeslot, is set to 1ms. For this AS3701A-BWLM-52 variant, the delay interval is disabled for all for timeslots.

The delay interval is defined with the bit <7> of fuse register a5h.

3.3 Reset Time

The reset time is the duration after timeslot 3 (GPIO2) where the XRES signel is still kept low and is set to 10ms.

The reset time is defined with the bits <5:4> of fuse register a7h.

3.4 Reset Voltage Rise

The Reset Voltage Rise level is set to 3.6V, whereby the Reset Voltage Fall level automatically jumps to a default value of 3.4V.

The reset voltage rise is defined with the bits <3:1> of fuse register a8h.

3.5 ON key

The ON key is defined as a push button and is configured as active high! This means the ON-key has to be forced to VSUP shortly to assert the ON-key function.
Furthermore the ON-key longpress is activated and a long press on the ON-key to VSUP for >4s initiates a Power-off of AS3701A!

The ON-key configuration is a combined definition of the bits <2:0> of fuse register a6h, the bit <0> of fuse register a8h and the bit <2> of fuse register a9h.

3.6 Auto-off

The Auto-off feature is activated!
This feature allows to force the PMIC directly into the Power-off state right after a power-up from scratch (first battery insertion or charger adapter insertion without battery). In this case, the PMIC will not enter the OTP startup stage!

The auto-off feature is defined with the bit <7> of fuse register a7h.

3.7 NTC-Input

For the AS3701A-BWLM-52 variant the NTC-input is defined with the XIRQ_NTC pin! This pin must be used to connect the NTC resistor of the battery.

The NTC-input is defined with the bits <1:0> of fuse register a9h.

3.8 USB Current Limit

The USB Current Limit of the internal pre-regulator is set to 470mA. Whenever a charger adapter is connected to the VUSB input, the input current into the PMIC is limited to 470mA!

The USB current limit is defined with the bits <7:4> of fuse register a7h.

3.9 Supply Reset Enable & Power Off at VSUP-low

Both bits are activated for the AS3701A-BWLM-52 variant, which forces the AS3701 into the Power OFF mode, when the Reset Voltage Fall level (3.4V) is reached!

The Supply Reset Enable feature is defined with the bit <3> of fuse register a9h and the Power OFF at VSUP-low is defined with the bit <1> of fuse register a7h.

4 OTP Fuse Register Setting for AS3701A-BWLM-52

Register 0xa5 = 0x40 (01000000b)
Register 0xa6 = 0x00 (00000000b)
Register 0xa7 = 0x8a (10001010b)
Register 0xa8 = 0x8f (10001111b)
Register 0xa9 = 0x0d (00001101b)
Register 0xaa = 0x91 (10010001b)
Register 0xab = 0x7e (01111110b)
Register 0xac = 0xaa (10101010b)
Register 0xad = 0x0a (00001010b)
Register 0xae = 0xdf (11011111b)
Register 0xaf = 0x00 (00000000b)

5 Ordering & Contact Information

Ordering Code	Marking	Quantity	Delivery Form	Package
AS3701A-BWLM-52	1V2-52	500pcs	T & R	20balls WL-CSP

Note: ams AG also supplies an evaluation board with a mounted AS3701B that can be altered with a software GUI.

With this software the user can determine the desired OTP setting for its application. Please contact ams for your OTP setting requirements. An alternative to the OTP programming is to start up an external uC and boot up AS3701B via the I2C commands.

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7 Revision Information

Changes from previous version to current revision 1-00 (2016-Dec-13)	Page
final version 1-00	

Note: Page numbers for the previous version may differ from page numbers in the current revision.
Correction of typographical errors is not explicitly mentioned.