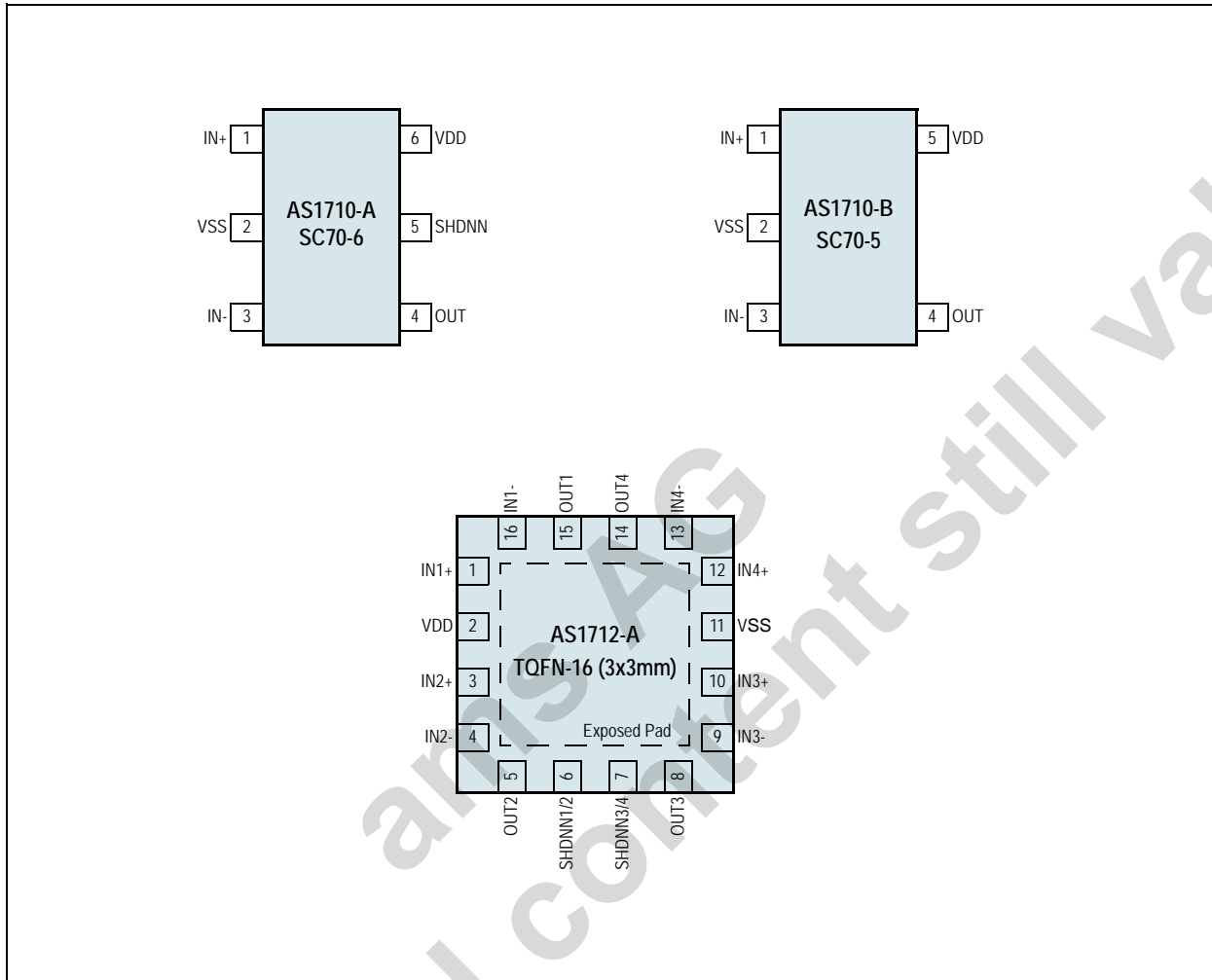




## 4 Pin Assignments

Figure 2. Pin Assignments (Top View)



### 4.1 Pin Descriptions

Table 2. Pin Descriptions

Pin Number	Pin Name	Description
See Figure 2	IN+	Non-inverting Input
	IN-	Inverting Input
	VDD	Positive Supply Input
	VSS	Negative Supply Input. This pin must be connected to ground in single-supply applications.
	SHDNN	Active Low Shutdown Control
	OUT	Amplifier Output
	Exposed Pad	Exposed Pad. This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation.

## 5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Electrical Characteristics on page 4](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments	
<b>Electrical Parameters</b>					
Supply Voltage (VDD to VSS)		+7	V		
Supply Voltage (All Other Pins)	VSS - 0.3	VDD + 0.3	V		
Output Short-Circuit Duration to VDD or VSS		1	s		
<b>Thermal Information</b>					
Continuous Power Dissipation	SC70-5		247	mW	Derate at 31mW/°C above 70°C
	SC70-6		245		
Thermal Resistance $\Theta_{JA}$	TQFN-16 (3x3mm)		33	°C/W	on PCB
<b>Temperature Ranges and Storage Conditions</b>					
Storage Temperature Range	-65	+150		°C	
Junction Temperature		+150		°C	
Package Body Temperature		+260		°C	The reflow peak soldering temperature (body temperature) specified is in accordance with <i>IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"</i> . The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85		%	
Moisture Sensitive Level		1			Represents a maximum floor life time of unlimited

## 6 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed by production tests or SQC (Statistical Quality Control) methods.

### 6.1 DC Electrical Characteristics

$V_{DD} = 2.7V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_{LOAD} = \text{Infinite}$ ,  $V_{SHDNN} = V_{DD}$ , Typical values at  $T_{AMB} = 25^{\circ}C$ .

Table 4. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	
TAMB	Operating Temperature Range		-40		+85	°C	
VDD	Supply Voltage Range	Inferred from Power Supply Rejection Ratio Test	2.7		5.5	V	
VOFFSET	Input Offset Voltage		-3	0.6	+3	mV	
IBIAS	Input Bias Current	$V_{CM} = V_{SS}$ to $V_{DD}$		50 <sup>1</sup>		pA	
IOFFSET	Input Offset Current	$V_{CM} = V_{SS}$ to $V_{DD}$		50 <sup>1</sup>		pA	
RIN	Input Resistance			1000 <sup>1</sup>		MΩ	
VCM	Common Mode Input Voltage Range	Inferred from Common Mode Rejection Ratio <sup>1</sup>	VSS		VDD	V	
CMRR	Common Mode Rejection Ratio	$V_{SS} < V_{CM} < V_{DD}$	-45	-70		dB	
PSRR	Power Supply Rejection Ratio	$V_{DD} = 2.7$ to $5.5V$	-70	-85		dB	
ROUT	Shutdown Output Impedance	$V_{SHDNN} = 0V$ (A-Versions)		130 <sup>1</sup>		Ω	
VOUT-SHDNN	Shutdown Output Voltage	$V_{SHDNN} = 0V$ , $R_{LOAD} = 2k\Omega$ to $V_{DD}$ (A-Versions)		170	300	mV	
AVOL	Large Signal Voltage Gain	$V_{SS} + 0.20V < V_{OUT} < V_{DD} - 0.20V$	$R_{LOAD} = 100k\Omega$	85	100	dB	
			$R_{LOAD} = 2k\Omega$	79	92		
			$R_{LOAD} = 200\Omega$	69	80		
VOUT	Output Voltage Swing	$V_{DD} - V_{OH}$ or $V_{OL} - V_{SS}$	$R_{LOAD} = 32\Omega$		350	650	mV
			$R_{LOAD} = 200\Omega$		70	120	
			$R_{LOAD} = 2k\Omega$		9	20	
	Output Voltage	$V_{DD} - V_{OH}$ or $V_{OL} - V_{SS}$				mV	
			$I_{LOAD} = 10mA$ , $V_{DD} = 2.7V$	55	100		
			$I_{LOAD} = 30mA$ , $V_{DD} = 5V$	100	180		
IOUT	Output Source/Sink Current	$V_{DD} = 2.7V$ , $V_{-} = V_{CM}$ , $V_{+} = V_{CM} \pm 100mV$		100		mA	
		$V_{DD} = 5.0V$ , $V_{-} = V_{CM}$ , $V_{+} = V_{CM} \pm 100mV$		200			
IDD	Quiescent Supply Current per Op Amp Output	$V_{DD} = 2.7V$ , $V_{CM} = V_{DD}/2$		1.6	3.2	mA	
		$V_{DD} = 5.0V$ , $V_{CM} = V_{DD}/2$		2.3	4.6		
IDD-SHDNN	Shutdown Supply Current per Op Amp (A-Versions)	$V_{SHDNN} = 0V$	$V_{DD} = 2.7V$	1	2000 <sup>1</sup>	nA	
	SHDNN Logic Threshold (A-Versions)	Shutdown Mode			$V_{SS} + 0.3$	V	
		Normal Operation			$V_{DD} - 0.3$		
	SHDNN Input Bias Current	$V_{SS} < V_{SHDNN} < V_{DD}$ (A-Versions)			50 <sup>1</sup>	pA	

1. Guaranteed by design.

## 6.2 AC Electrical Characteristics

$V_{DD} = 2.7V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_{LOAD} = \text{Infinite}$ ,  $V_{SHDNN} = V_{DD}$ , Typical values at  $T_{AMB} = 25^{\circ}C$ .

Table 5. AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
GBWP	Gain-Bandwidth Product	$V_{CM} = V_{DD}/2$		10		MHz
FPBW	Full-Power Bandwidth	$V_{OUT} = 2V_{P-P}$ , $V_{DD} = 5V$		2.5		MHz
SR	Slew Rate			10		V/ $\mu$ s
PM	Phase Margin			70		deg
GM	Gain Margin <sup>1</sup>			15		dB
THD+N	Total Harmonic Distortion Plus Noise	$f = 10kHz$ , $V_{OUT} = 2V_{P-P}$ , $AV_{CL} = 1V/V$		0.05		%
CIN	Input Capacitance			6		pF
en	Voltage-Noise Density <sup>1</sup>	$f = 1kHz$		15		nV/ $\sqrt{Hz}$
		$f = 10kHz$		10		
	Capacitive-Load Stability	$AV_{CL} = 1V/V$ , no sustained oscillations		100		pF
tSHDN	Shutdown Time (AS1710A)			1		$\mu$ s
tENABLE	Enable Time from Shutdown (AS1710A)			7		$\mu$ s
tON	Power-Up Time			20		ns

1. Guaranteed by design.

## 7 Typical Operating Characteristics

$V_{DD} = 2.7V$ ;  $V_{SS} = 0V$ ;  $V_{CM} = V_{DD}/2$ ;  $V_{OUT} = V_{DD}/2$ ;  $R_{LOAD} = \infty$ ;  $V_{SHDN} = V_{DD}$   $T_{AMB} = +25^{\circ}C$  (unless otherwise specified).

Figure 3. Gain and Phase vs. Frequency

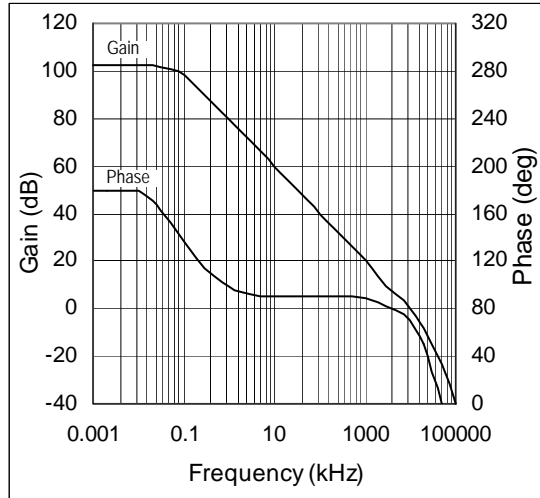


Figure 4. Gain and Phase vs. Frequency,  $C_{LOAD} = 100pF$

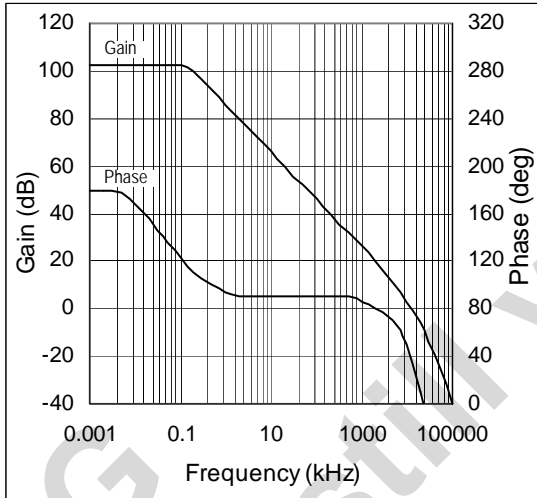


Figure 5. PSRR vs. Frequency

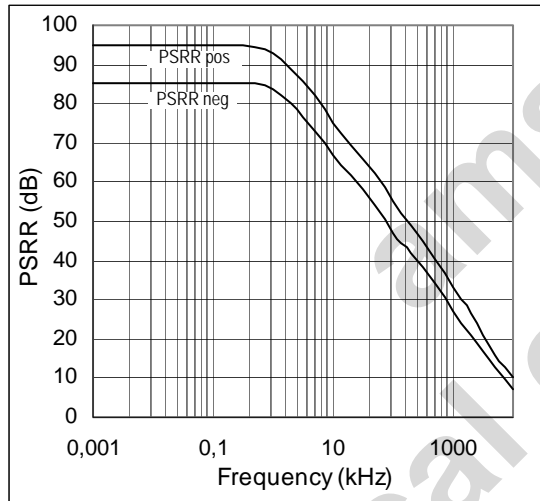


Figure 6. CMRR vs. Frequency

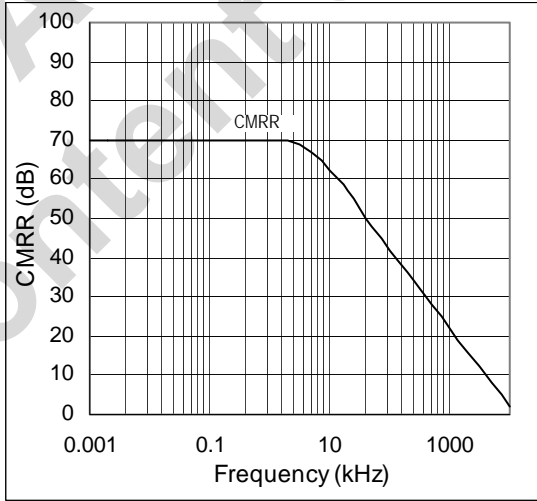


Figure 7. Supply Current vs. Temperature

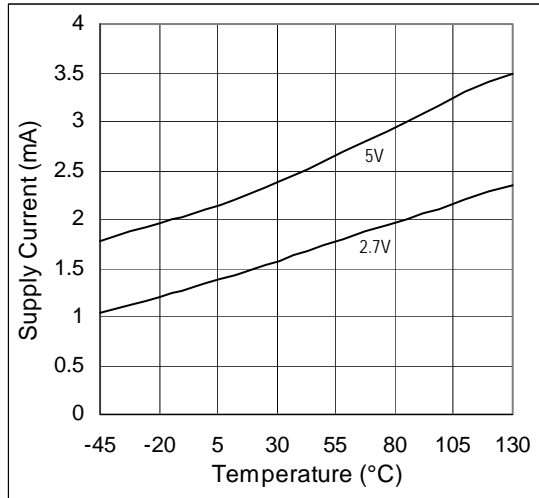


Figure 8. Shutdown Current vs. Temperature

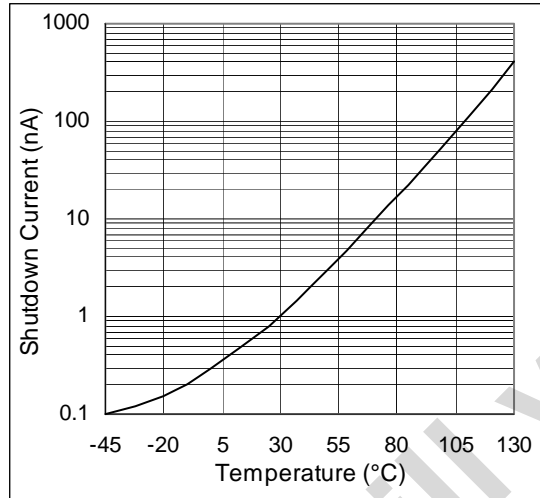


Figure 9. Supply Current vs. Common-Mode Voltage

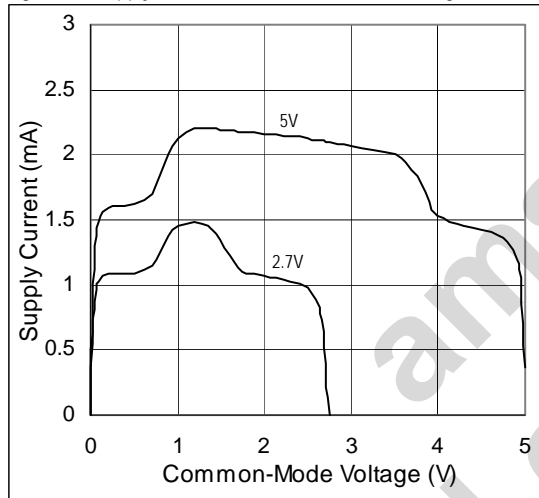


Figure 10. Input Voltage Noise vs. Frequency

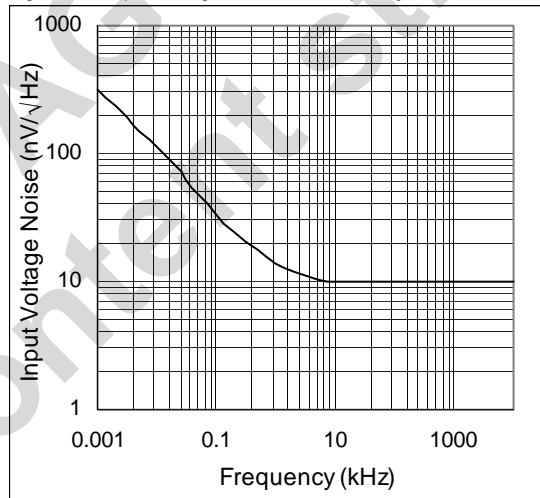


Figure 11. Output Voltage vs. Output Current, sourcing

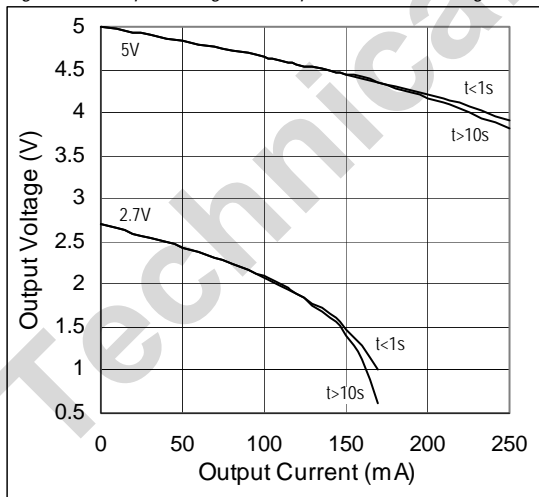


Figure 12. Output Voltage vs. Output Current, sinking

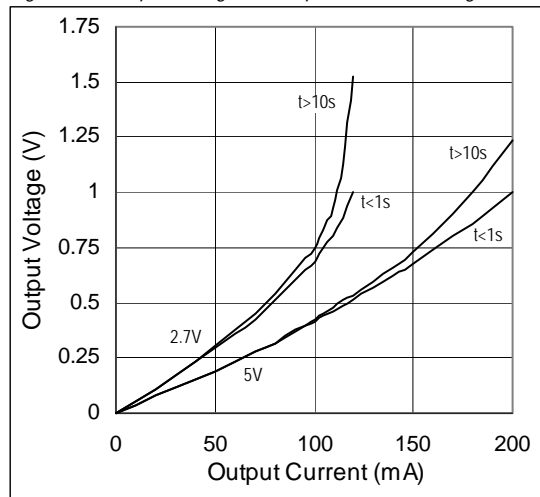


Figure 13. Output Swing High vs. Temperature

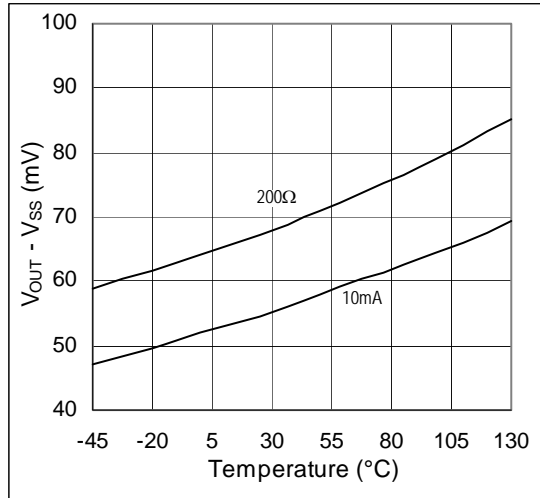


Figure 14. Output Swing Low vs. Temperature

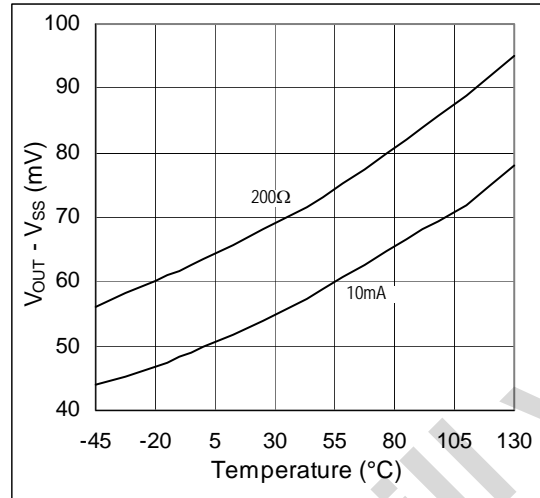


Figure 15. Transient Response, 100mV, 10pF load

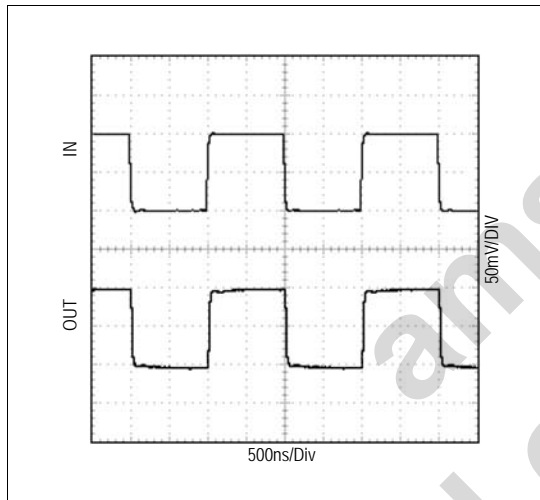


Figure 16. Transient Response, 100mV, 100pF load

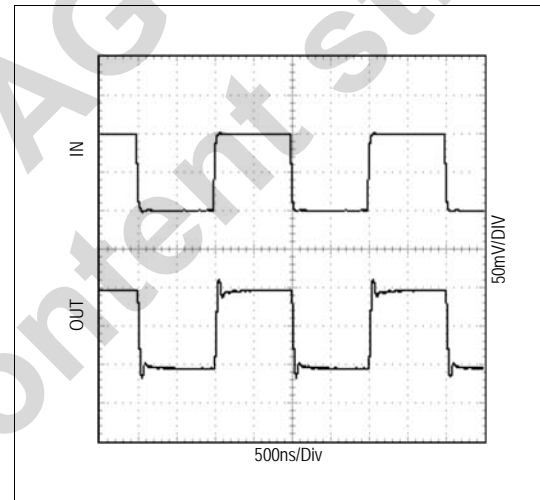


Figure 17. Transient Response, 1V, 10pF load

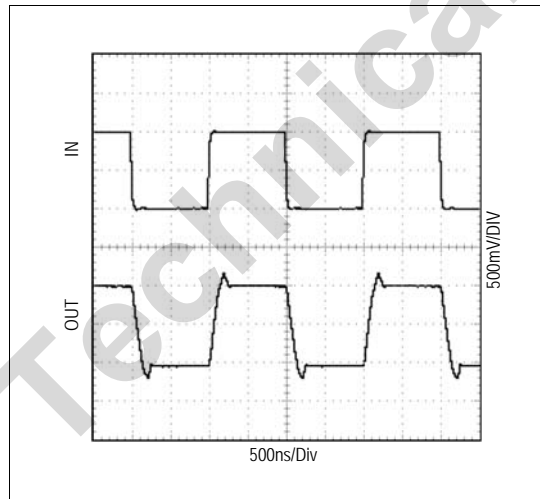


Figure 18. Transient Response, 1V, 100pF load

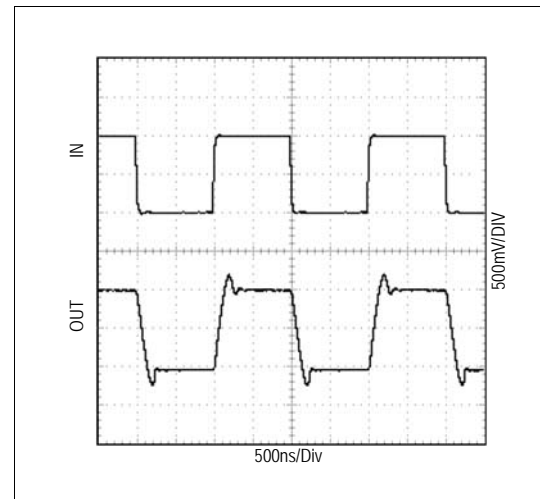




Figure 19. Transient Response, 2V, 10pF load

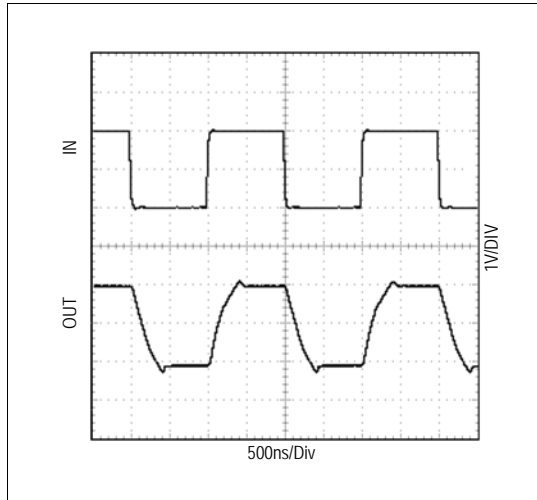
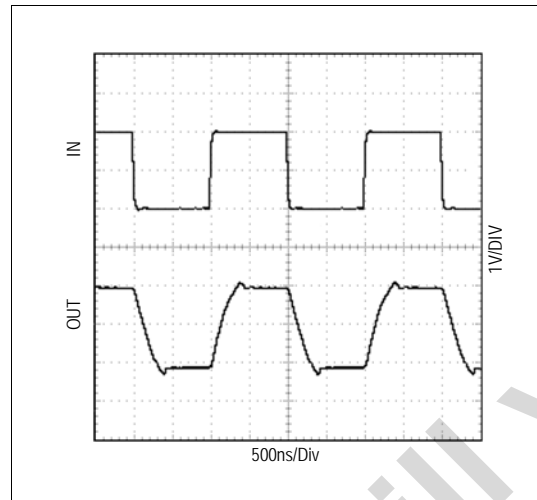


Figure 20. Transient Response, 2V, 100pF load



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## 8 Application Information

### 8.1 Package Power Dissipation

**Caution:** Due to the high output current drive, this op-amp can exceed the absolute maximum power-dissipation rating. Normally, when peak current is less than or equal to 40mA the maximum package power dissipation is not exceeded for any of the package types offered.

The absolute maximum power-dissipation rating of each package should always be verified. (EQ 1) gives an approximation of the package power dissipation:

$$P_{\text{PACKAGEDISS}} \cong V_{\text{RMS}} I_{\text{RMS}} \cos\theta \quad (\text{EQ 1})$$

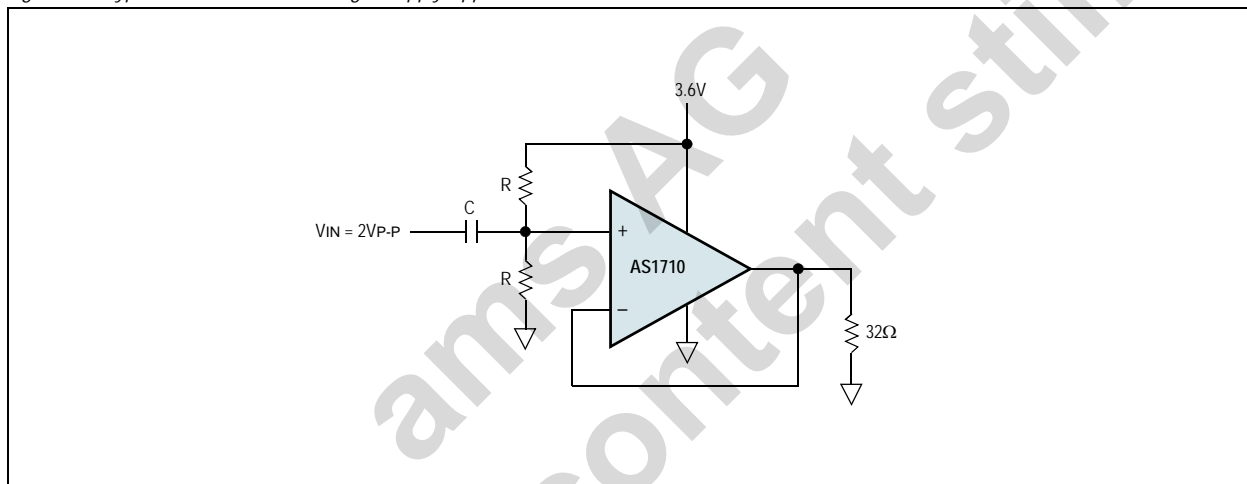
**Where:**

$V_{\text{RMS}}$  is the RMS voltage from  $V_{\text{DD}}$  to  $V_{\text{OUT}}$  when sourcing current, and from  $V_{\text{OUT}}$  to  $V_{\text{SS}}$  when sinking current.

$I_{\text{RMS}}$  is the RMS current flowing in or out of the op-amp and the load.

$\theta$  is the phase difference between the voltage and the current. For resistive loads,  $\cos\theta = 1$ .

Figure 21. Typical AS1710/AS1712 Single-Supply Application



$V_{\text{RMS}}$  can be calculated as:

$$V_{\text{RMS}} \cong (V_{\text{DD}} - V_{\text{DC}}) + V_{\text{PEAK}} / \sqrt{2} \quad (\text{EQ 2})$$

**Where:**

$V_{\text{DC}}$  is the DC component of the output voltage.

$V_{\text{PEAK}}$  is the highest positive excursion of the AC component of the output voltage.

For the circuit shown in Figure 21:

$$V_{\text{RMS}} = (3.6\text{V} - 1.8\text{V}) + 1.0\text{V} / \sqrt{2} = 2.507\text{VRMS}$$

$I_{\text{RMS}}$  can be calculated as:

$$I_{\text{RMS}} \cong I_{\text{DC}} + (I_{\text{PEAK}} / \sqrt{2}) \quad (\text{EQ 3})$$

**Where:**

$I_{\text{DC}}$  is the DC component of the output current.

$I_{\text{PEAK}}$  is the highest positive excursion of the AC component of the output current.

For the circuit shown in Figure 21:

$$I_{\text{RMS}} = (1.8\text{V} / 32\Omega) + (1.0\text{V} / 32\Omega) / \sqrt{2} = 78.4\text{mARMS}$$

Therefore, for the circuit in Figure 21 the package power dissipation can be calculated as:

$$P_{\text{PACKAGEDISS}} = V_{\text{RMS}} I_{\text{RMS}} \cos\theta = 196\text{mW}$$

Adding a coupling capacitor improves the package power dissipation because there is no DC current to the load, as shown in Figure 22 on page 11.



















