TSL4531

Digital Ambient Light Sensor

General Description

The TSL4531 family of devices provides ambient light sensing (ALS) that approximates human eye response under a variety of lighting conditions. The devices have three selectable integration times and provide a direct 16-bit lux output via an I^2C bus interface. The wide dynamic range of the ALS makes it particularly useful in outdoor applications where it is exposed to direct sunlight. The device is ideal for use in automatic control of street lights and security, billboard, and automotive lighting. The TSL4531 devices can also be used in solid state and general lighting for automatic control and daylight harvesting to maximize energy conservation. Other applications include display backlight control to extend battery life and optimize visibility in cell phones, tablets, and notebooks.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of this device are listed below:

Figure 1:
Added Value of Using TSL4531

Benefits	Features
• Requires no Lux Equation Software Calculations	• Simple Direct Lux Output
• Enables Automatic Display Brightness Control for Reduced Total System Power Consumption	• Approximates Human Eye Response in Diverse Lighting Conditions
• Enables Application Versatility in Varying Lighting Environments	• Three User-Selectable Integration Times (100 ms, 200 ms and 400 ms)
• Enables 3 Lux to 220k Lux Bright Sunlight Operation	• Wide Dynamic Range
• Multiple Integration Times Enables the Rejection of 50 Hz/60 Hz Lighting Ripples	• Rejects 50 Hz/60 Hz Lighting Ripple
• Enabling a Low Active and Power-Down Modes Reduces Average Power Consumption	• Low Active Current (110 µA typical) with Power Down Mode (2.2 µA typical) Enables *Green* Products
• Digital Interfaces are Less Susceptible to Noise	• 16-bit Digital Output with I^2C Compatibility
• Reduces Board Space Requirements while Simplifying Designs	• Ultra-Small 2 mm × 2 mm ChipLED (CL) Package
• 2.5 V Power Rail Enables Low-Power Operation	• 2.5-V Supply Voltage with 1.8-V Logic Interface

Applications

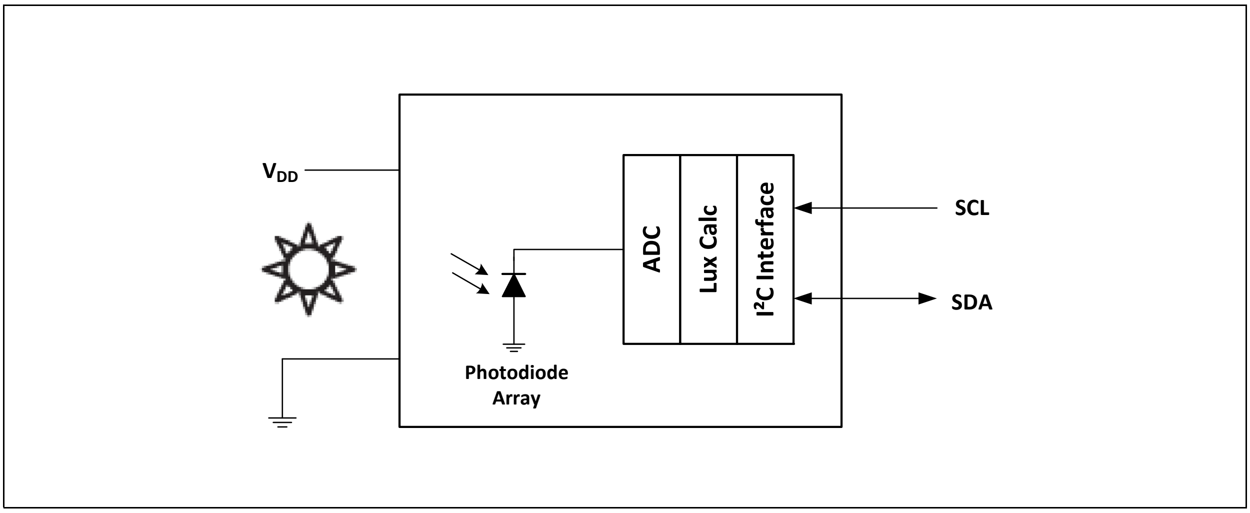
The applications of TSL4531 include:

- Outdoor Lighting Control
  - Street Lights
  - Security Lights
  - Traffic Signals
  - Commercial Billboards
- Display Backlight Control
  - Automotive Instrumentation
  - Cell Phones
  - Tablets and Notebooks
- Solid-State and General Lighting and Daylight Harvesting
  - Commercial Lighting
  - Industrial Lighting

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Block Diagram



Detailed Description

The device contains a photodiode array, an integrating analog-to-digital converter (ADC), signal processing circuitry, lux calculation logic, and an I²C serial interface on a single CMOS integrated circuit to provide lux data with a 16-bit output. No external circuitry is required for signal conditioning. The device features power management modes where the user can select continuous operation mode, single data acquisition cycle operation mode, and power savings mode by which the device enters a power savings state between data acquisitions. The device has three user-selectable integration times of 100 ms, 200 ms, or 400 ms, allowing the user to adjust the sensitivity of the device.

Pin Assignment

The TSL4531 pin assignments are described below.

Figure 3:
Pin Diagram

Package CL ChipLED (Top View):
Package drawing is not to scale.

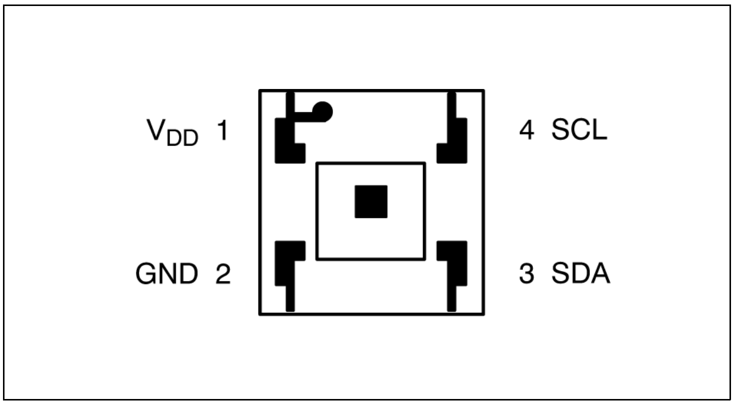


Figure 4:
Pin Description

Pin Number	Pin Name	Pin Type	Description
1	V_{DD}		Supply voltage.
2	GND		Power supply ground. All voltages are referenced to GND.
3	SDA	Input/Output	I^2C serial data I/O terminal — bidirectional.
4	SCL	Input	I^2C serial clock input terminal.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)

Parameter	Min	Max	Units	Comments
Supply voltage, V_{DD}		4.5	V	All voltages are with respect to GND
Input terminal voltage	−0.5	4.5	V	
Output terminal voltage	−0.5	4.5	V	
Output terminal current	−1	20	mA	
Storage temperature range, T_{stg}	−40	85	°C	
ESD tolerance, human body model	±2000		V	

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Unit
V_{DD}	Supply voltage	2.3	2.5	3.3	V
T_A	Operating free-air temperature	-15		70	°C

Figure 7:
Operating Characteristics, V_{DD} = 2.5 V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Supply current	Active (1)		110	130	µA
		Power down — no I²C activity		2.2	4	
I_{LEAK}	Leakage current, SDA and SCL pins		-5		5	µA
V_{IH}	SCL, SDA input high voltage	TSL45311, TSL45315	0.7 V_{DD}			V
		TSL45313, TSL45317	1.25			
V_{IL}	SCL, SDA input low voltage	TSL45311, TSL45315			0.3 V_{DD}	V
		TSL45313, TSL45317			0.54	

Note(s):

1. The average supply current will be slightly lower when PSAVESKIP = 0.

Figure 8:
ALS Characteristics, V_{DD} = 2.5 V, T_A = 25°C, TCNTRL = 1× (Tint = 400 ms) (unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC count range		0		65535	counts
ADC count value	λ_p = white LED, CCT = 4000K, E_V = 1000 lux		1000		counts
	λ_p = 880 nm + 940 nm, E_e = 345 µW/cm^2 (1)			3	
ADC count value ratio	Inc std A/Fluorescent F12 (2) (4)	80		120	%
Sensor output responsivity	λ_p = white LED, CCT = 4000K	0.8	1	1.2	count/ lux
Dynamic range	Incandescent light source: STD A (3) (4)	3		220k	lux
Temperature coefficient	-15°C to 0°C	-0.25		0	% / °C
	0°C to 70°C	-0.20		0	
Integration time	TCNTRL = 10	96	100	104	ms
	TCNTRL = 01	192	200	208	
	TCNTRL = 00	384	400	416	
Total cycle time	TCNTRL = 10, PSAVESKIP = 0 (5)	110.4	115	119.6	ms
	TCNTRL = 01, PSAVESKIP = 0 (5)	220.8	230	239.2	
	TCNTRL = 00, PSAVESKIP = 0 (5)	441.6	460	478.4	

Note(s):

1. Combination of IR LEDs used with peak wavelengths of 880 nm and 940 nm for IR rejection production test.
2. Incandescent STD A light source at 300 lux. Fluorescent F12 light source at 300 lux.
3. 220k lux reading possible with TCNTRL set to 4× MULTIPLIER (Tint = 100 ms).
4. Not tested in production.
5. When PSAVESKIP = 1, total cycle time equals integration time.

Timing Characteristics

The timing characteristics of TSL4531 are given below.

Figure 9:
AC Electrical Characteristics, V_{DD} = 2.5 V, T_A = 25°C (unless otherwise noted)

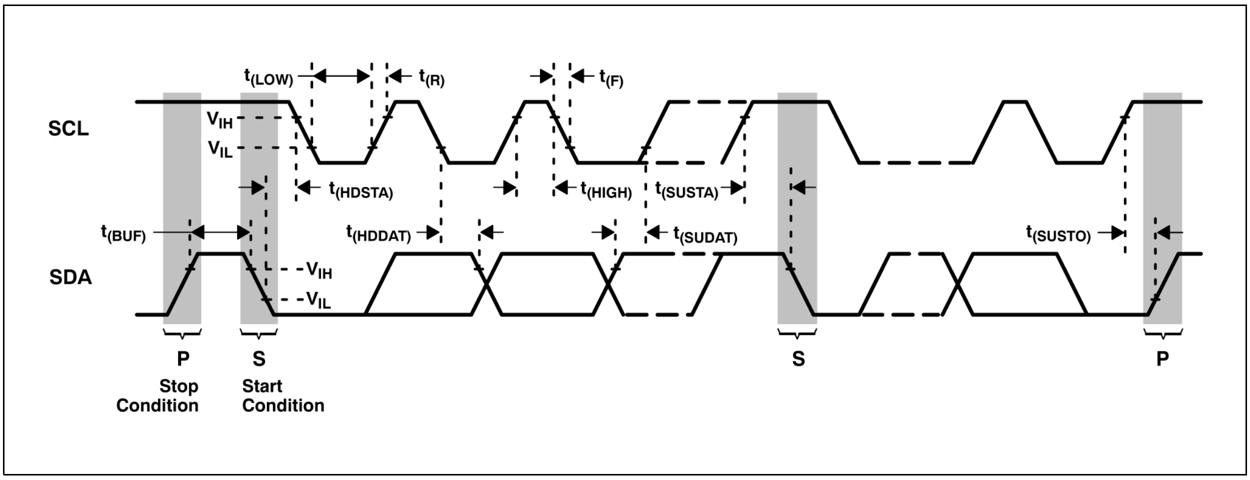
Parameter (1)	Description	Min	Max	Units
$f_{(SCL)}$	Clock frequency		400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition	4.7		µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	4		µs
$t_{(SUSTA)}$	Repeated start condition setup time	4.7		µs
$t_{(SUSTO)}$	Stop condition setup time	4		µs
$t_{(HDDAT)}$	Data hold time	300		ns
$t_{(SUDAT)}$	Data setup time	250		ns
$t_{(LOW)}$	SCL clock low period	4.7		µs
$t_{(HIGH)}$	SCL clock high period	4		µs
$t_{(TIMEOUT)}$	Detect clock/data low timeout	25	35	ms
$t_{(F)}$	Clock/data fall time		300	ns
$t_{(R)}$	Clock/data rise time		1000	ns
C_i	Input pin capacitance		10	pF

Note(s):

1. Specified by design and characterization – not production tested.

Timing Diagrams

Figure 10:
Parameter Measurement Information



Typical Operating Characteristics

Figure 11:
Normalized Spectral Responsivity

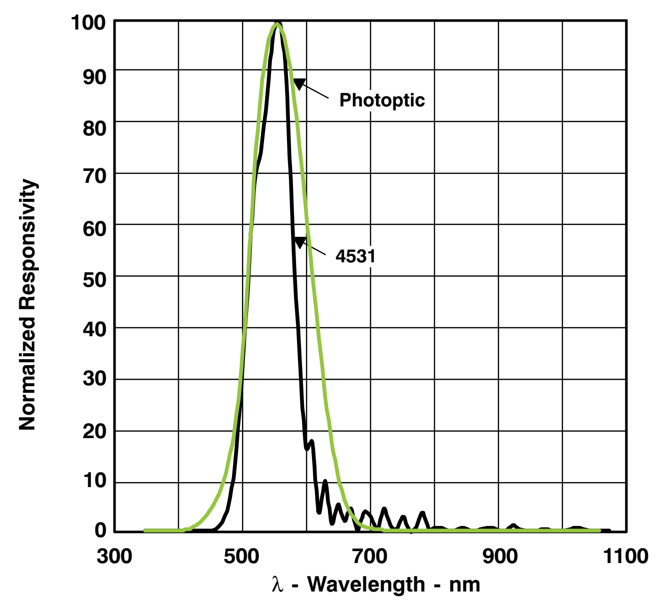


Figure 12:
Normalized Responsivity vs. Angular Displacement - CL Package

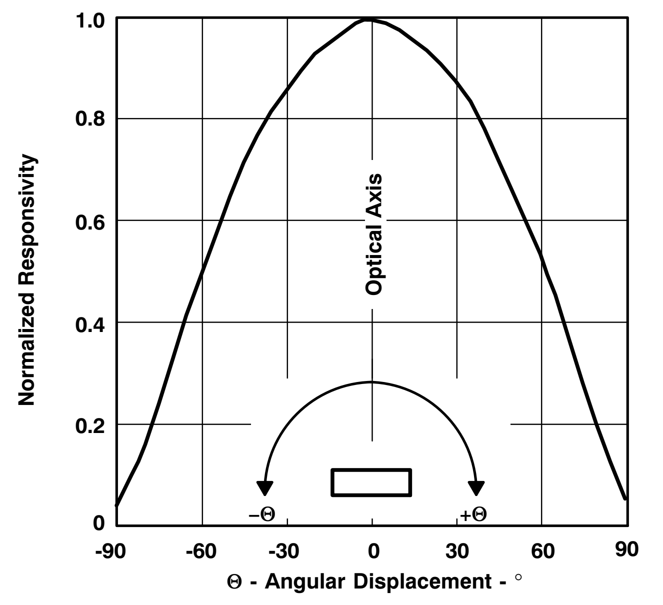


Figure 13:
I_{DD} vs. V_{DD}

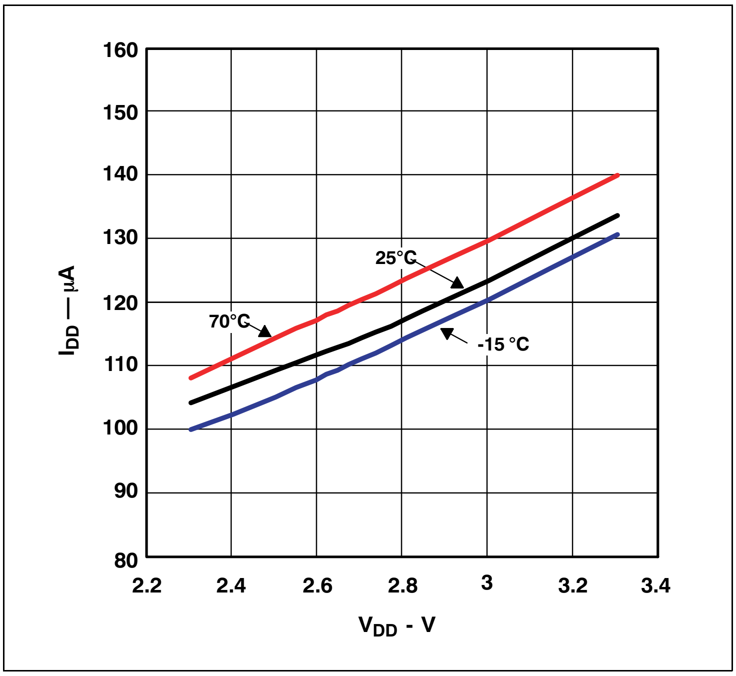
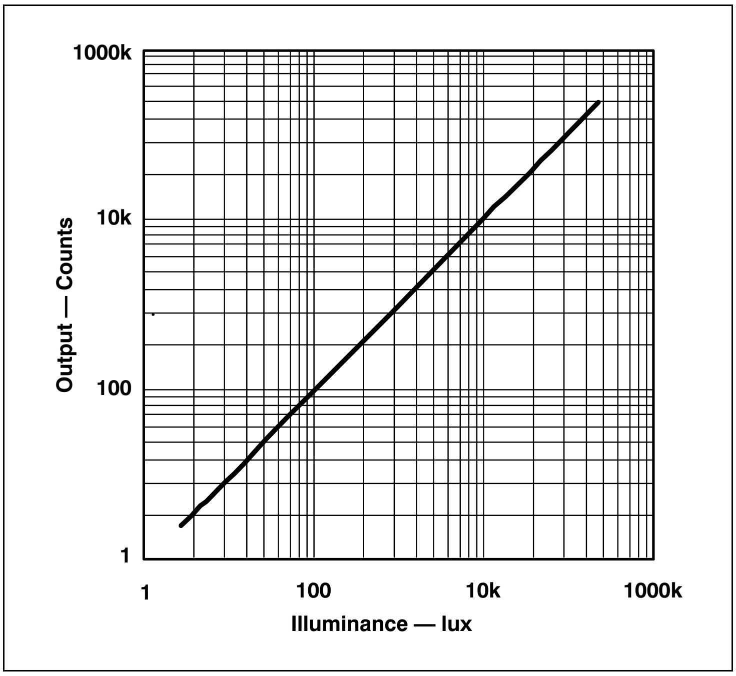


Figure 14:
Output vs. Illuminance



Principles of Operation

Analog-to-Digital Converter

The TSL4531 contains one integrating analog-to-digital converter (ADC) that integrates the current from the photodiode array. Upon completion of the conversion cycle, the conversion result is transferred to the data registers. Transfers are double-buffered to ensure that invalid data is not read during the transfer. After the transfer, the device will either automatically begin another integration cycle, or enter power-down mode, depending upon the mode setting in the control register.

The device features several key power management features. The mode of operation can be controlled to provide either continuous operation or single acquisition operation followed by a power-down state. In the continuous operation, a secondary mode can be enabled allowing the device to go into a low-power state in between each acquisition cycle.

The device allows the user to control the integration time. This enables the user to control the sensitivity of the device to allow for the greater dynamic range needed in bright lighting conditions such as sunlight. Integration times of 400 ms, 200 ms, or 100 ms are available. All integration times are multiples of 50 ms, allowing rejection of 50/60-Hz ripple present in a typical fluorescent lights. The lux output needs to be scaled depending on the integration time as shown in the calculating lux section.

Calculating Lux

The ADC output is a 16-bit number that is directly proportional to the value that approximates the human eye response in the commonly used illuminance unit of lux. The light level can be calculated using the following expression.

Light Level (lux) = MULTIPLIER × [(DATAHIGH << 8) + DATALOW]

Where:

MULTIPLIER = 1 for TCNTRL = 00 (Tint = 400 ms),
MULTIPLIER = 2 for TCNTRL = 01 (Tint = 200 ms), and
MULTIPLIER = 4 for TCNTRL = 10 (Tint = 100 ms), and
<< 8 indicates a logical 8-bit shift left operation, and
TCNTRL is a 2-bit field in the configuration register (0x01)

Example:

MULTIPLIER = 1
DATALOW = 0x9C
DATAHIGH = 0x63

Illuminance =

= 1 × [(DATAHIGH << 8) + DATALOW] lux
= (0x63 << 8) + 0x9C lux
= 0x639C lux
= 25500 lux

I²C Protocol

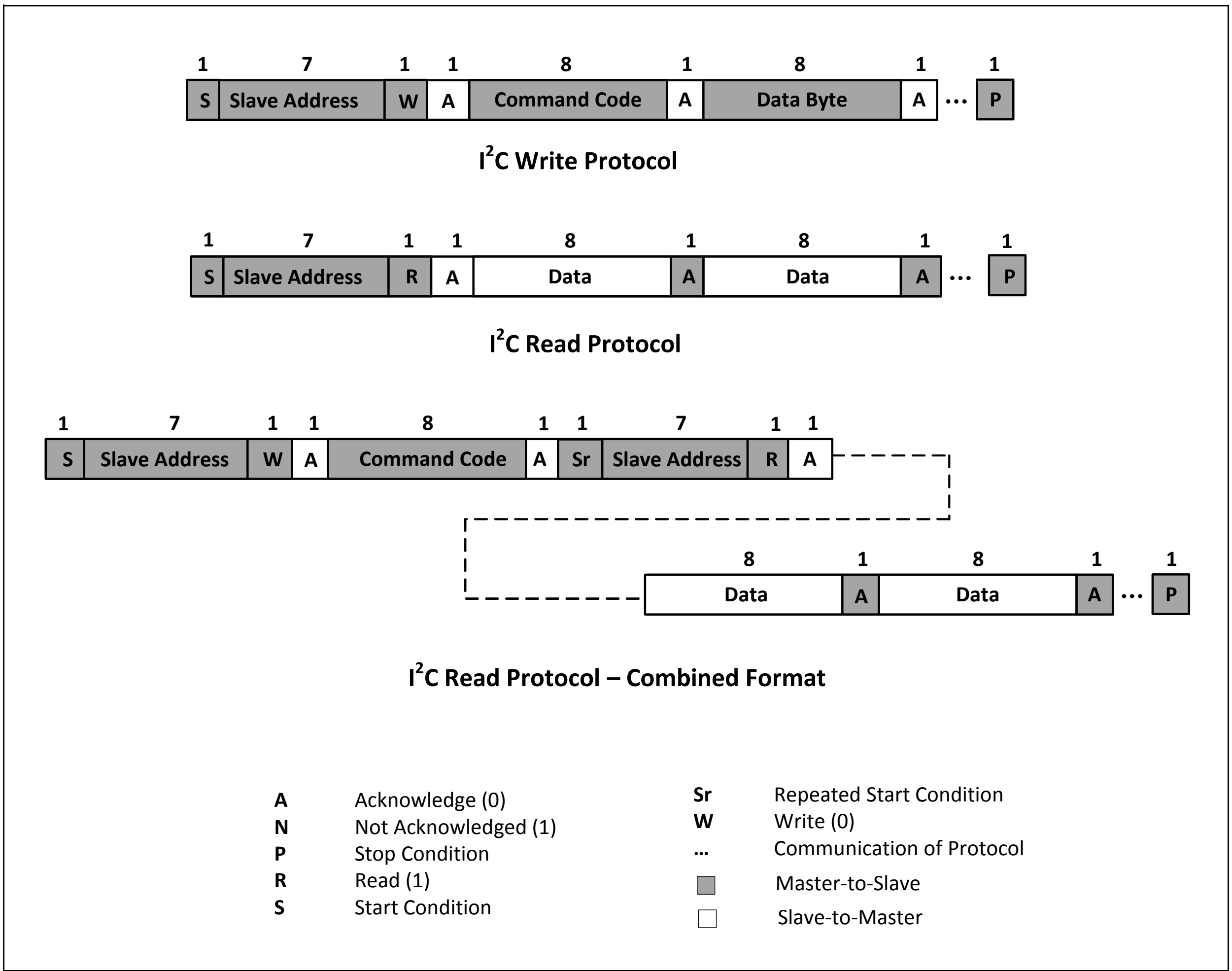
Interface and control are accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I²C addressing protocol.

The I²C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 15). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at:

http://www.i2c-bus.org/references/.

Figure 15:
I²C Protocols



Register Description

The device is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions.

Figure 16:
Register Set

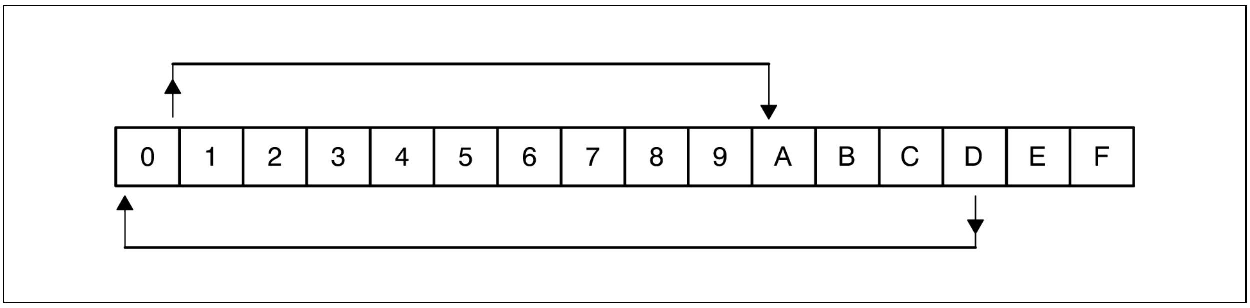
Address	Register Name	R/W	Register Function	Reset Value
--	COMMAND	W	Specifies register address	0x00
0x00	CONTROL	R/W	Power ON/OFF and single cycle	0x00
0x01	CONFIG	R/W	Powersave Enable / Integration Time	0x00
0x04	DATALOW	R	ALS Data LOW Register	0x00
0x05	DATAHIGH	R	ALS Data HIGH Register	0x00
0x0A	ID	R	Device ID	ID

The mechanics of accessing a specific register depends on the specific protocol used (see I²C Protocol). In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

There are 16 register locations, but only 5 registers are implemented. To make the register read process more efficient when reading multiple bytes of data as in the combined format protocol, the address index pointer is automatically incremented to skip over the unused registers, as shown in Figure below.

Address in hex
Address increments by 1 except where noted:
Cycle is 0h, Ah, Bh, Ch, Dh, 0h

Figure 17:
Combined Format Read Cycle Pattern



Command Register

The COMMAND register specifies the address of the target register for future write and read operations. It contains two user fields as described below and defaults to 0x00 at power-on.

Figure 18:
Command Register

7	6	5	4	3	2	1	0
COMMAND	Reserved			ADDRESS			

Fields	Bits	Description
COMMAND	7	Select Command Register. Must write as 1.
Reserved	6:4	Reserved. Write as 0.
ADDRESS	3:0	Address register. Selects the specific register for write and read transactions that follow.

Control Register (0x00)

The CONTROL register is used to power the device ON/OFF and single cycle.

Figure 19:
Control Register

7	6	5	4	3	2	1	0
Reserved						MODE	

<table>
<tr><th>Fields</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td>Reserved</td><td>7:2</td><td colspan="2">Reserved. Write as 0.</td></tr>
<tr><td rowspan="6">MODE</td><td rowspan="6">1:0</td><td colspan="2">Operating Mode. This two-bit field controls the mode of the device:</td></tr>
<tr><td>Field Value</td><td>Function</td></tr>
<tr><td>00</td><td>Power Down</td></tr>
<tr><td>01</td><td>Reserved</td></tr>
<tr><td>10</td><td>Run a single ADC cycle and return to PowerDown</td></tr>
<tr><td>11</td><td>Normal Operation</td></tr>
</table>

Configuration Register (0x01)

The CONFIGURATION register controls the integration timer and power saving enabling through two user fields.

Figure 20:
Configuration Register

7	6	5	4	3	2	1	0
Reserved				PSAVESKIP	Reserved	TCNTRL	

<table>
<tr><th>Fields</th><th>Bits</th><th colspan="3">Description</th></tr>
<tr><td>Reserved</td><td>7:4</td><td colspan="3">Reserved. Write as 0.</td></tr>
<tr><td>PSAVESKIP</td><td>3</td><td colspan="3">PowerSave Mode. When asserted, the power save states are skipped following a light integration cycle for shorter sampling rates [(1)].</td></tr>
<tr><td>Reserved</td><td>2</td><td colspan="3">Reserved. Write as 0.</td></tr>
<tr><td rowspan="6">TCNTRL</td><td rowspan="6">1:0</td><td colspan="3">Timer Control sets the integration time.</td></tr>
<tr><td>Field Value</td><td>Multiplier</td><td>Purpose</td></tr>
<tr><td>00</td><td>1×</td><td>T_{int} = 400 ms</td></tr>
<tr><td>01</td><td>2×</td><td>T_{int} = 200 ms</td></tr>
<tr><td>10</td><td>4×</td><td>T_{int} = 100 ms</td></tr>
<tr><td>11</td><td>--</td><td>Reserved</td></tr>
</table>

Note(s):

1. When PSAVESKIP = 0, the typical total cycle time is T_{int} + (60/MULTIPLIER) ms. When PSAVESKIP = 1, the typical total cycle time is T_{int}.

ALS Data Registers (0x04 - 0x05)

The ADC data is expressed as a 16-bit word stored in two 8-bit registers. The read-only ADC data registers DATALOW and DATAHIGH provide the low and high bytes, respectively, of the 16-bit ADC conversion value. The conversion value translates directly to units of lux.

Figure 21:
ALS Data Registers

Register	Address	Bits	Description
DATALOW	0x04	7:0	ADC conversion low byte
DATAHIGH	0x05	7:0	ADC conversion high byte

ID Register (0x0A)

The ID register is a read-only register that provides the value for the part number. The PARTNO field indicates the part number of each device given in the Available Options section and will remain constant.

Figure 22:
ID Register

7	6	5	4	3	2	1	0
PARTNO				Reserved			

Fields	Bits	Description	
PARTNO	7:4	**Field Value**	**Device Part Number**
		1000	TSL45317
		1001	TSL45313
		1010	TSL45315
		1011	TSL45311
Reserved	3:0	Reserved	

The ID register is useful for validating the device type and for verifying the functionality of the interface. When used for this purpose, it is recommended that the Reserved field be masked out as follows:

- Value = ID AND 0xF0
  where, AND represents a bit-wise AND function

Application Information: Hardware

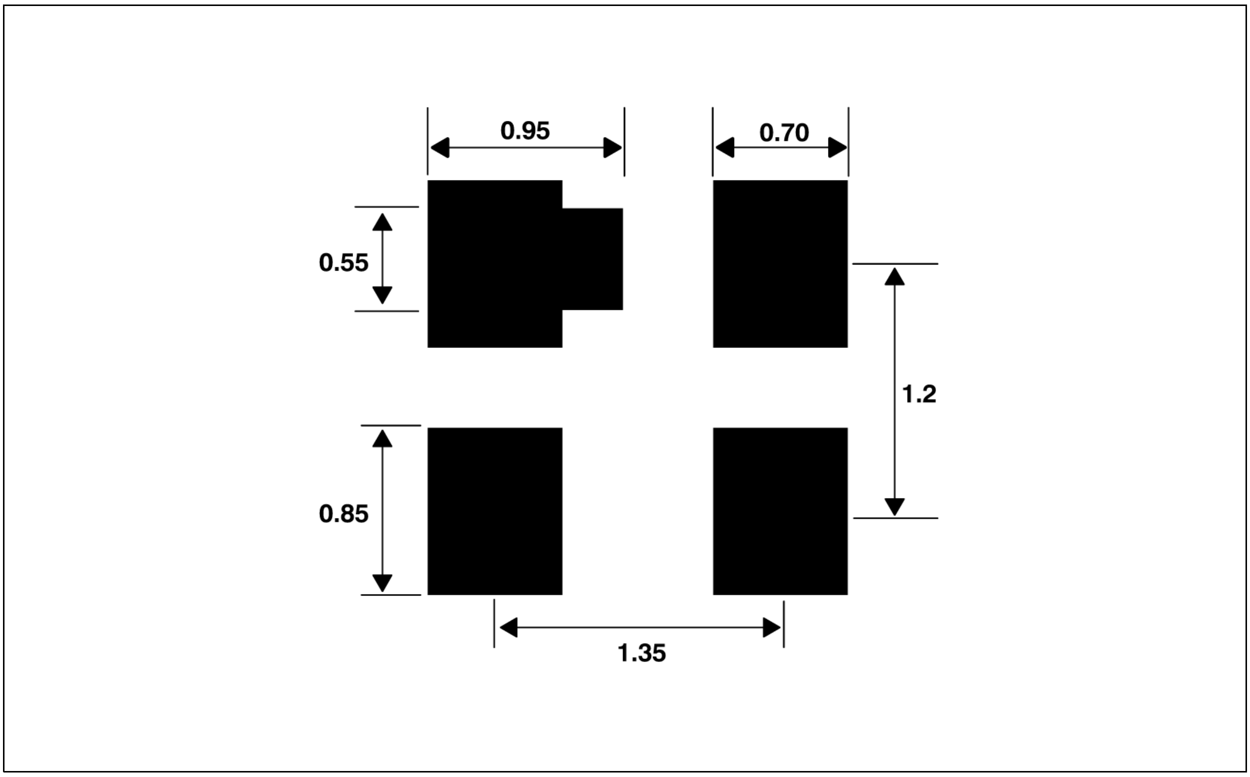
Power Supply Decoupling

The power supply lines must be decoupled with a 0.1-µF capacitor placed as close to the device package as possible. The bypass capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents caused by internal logic switching.

PCB Pad Layout

Suggested PCB pad layout guidelines for the CL package is shown in Figure 23.

Figure 23:
Suggested CL Package PCB Layout

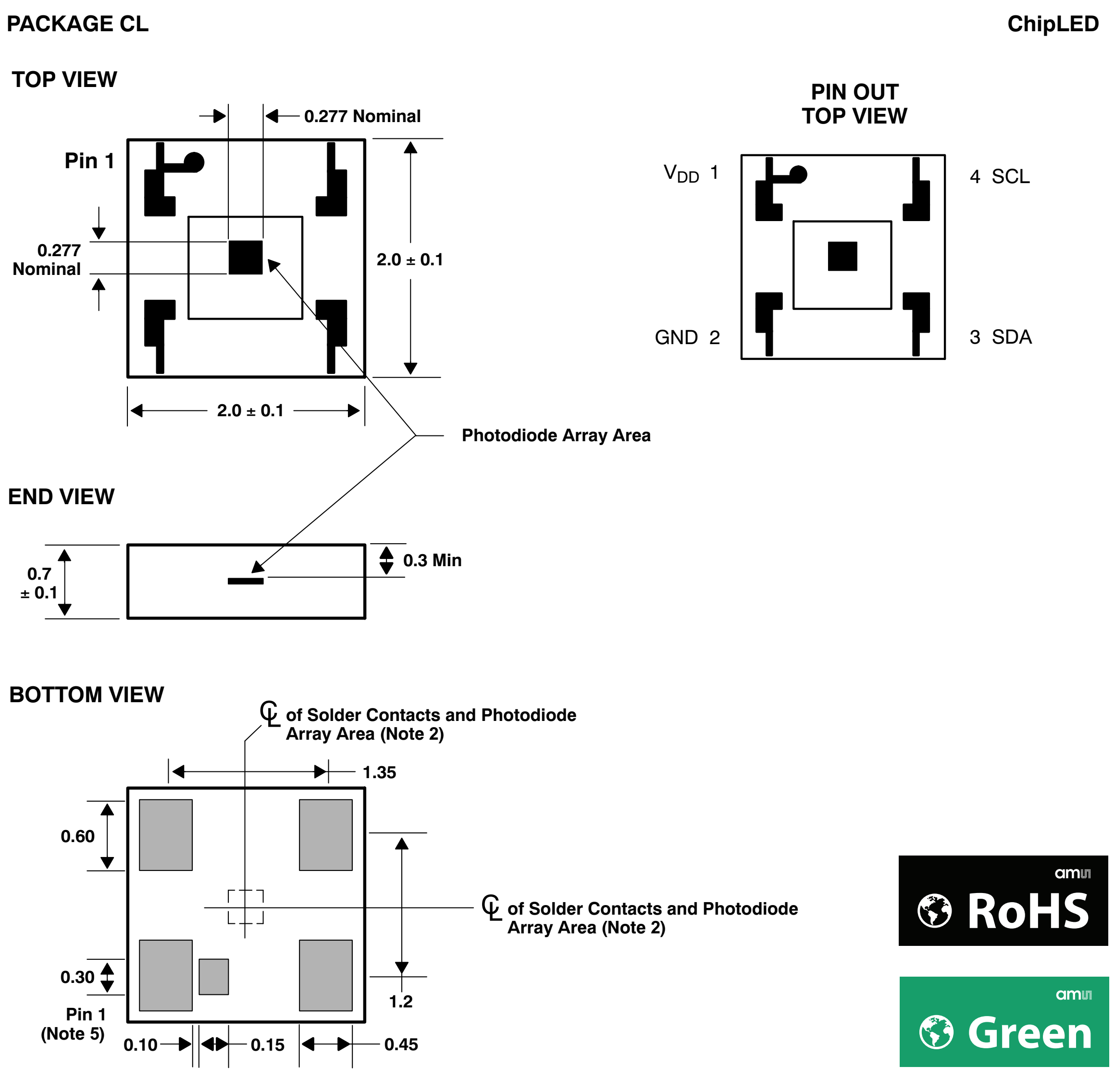


Note(s):

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Package Drawings & Markings

Figure 24:
Package CL − ChipLED Packaging Configuration

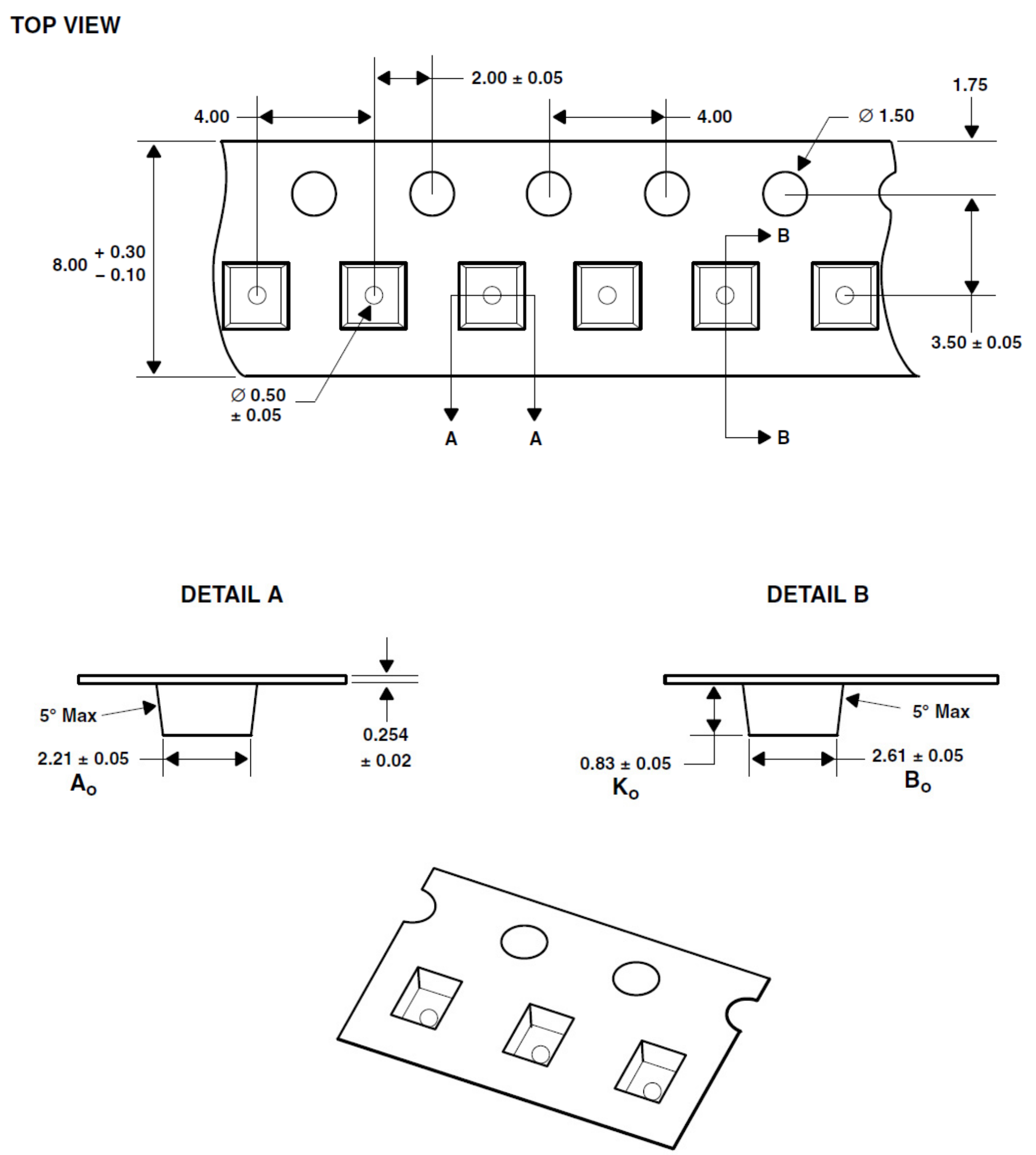


Note(s):

1. All linear dimensions are in millimeters.
2. The die is offset within the package to center the photodiode array to the solder contacts within a tolerance of ± 50 µm.
3. Package top surface is molded with an electrically nonconductive yellow clear plastic compound having an index of refraction of 1.55.
4. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
5. Bottom pin 1 indicator is electrically connected to pin 1.
6. This package contains no lead (Pb).
7. This drawing is subject to change without notice.

Carrier Tape & Reel Information

Figure 25:
Package CL Carrier Tape



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A_O, B_O, and K_O are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is 178 millimeters in diameter and contains 3500 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481-B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Soldering & Storage Information

Soldering Information

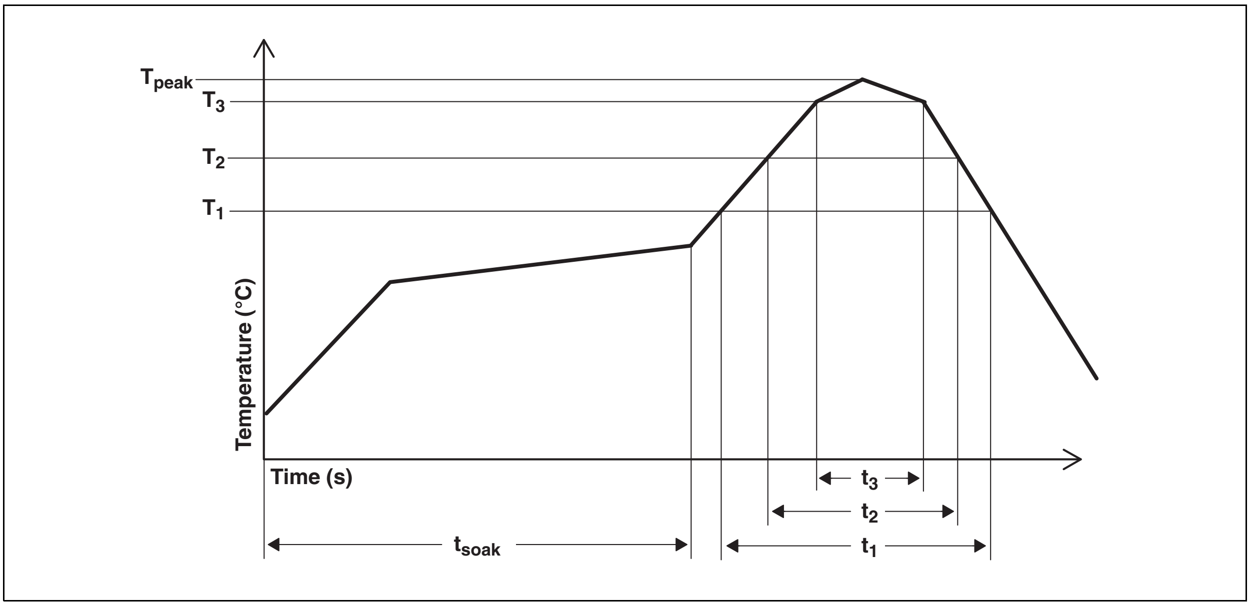
The CL package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 26:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5°C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T_1)	t_1	Max 60 s
Time above 230°C (T_2)	t_2	Max 50 s
Time above T_{peak} -10°C (T_3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max -5°C/s

Figure 27:
Solder Reflow Profile Graph



Note(s):
1. Not to scale – for reference only.

Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: < 40°C
- Relative Humidity: < 90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The CL package has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: < 30°C
- Relative Humidity: < 60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 28:
Ordering Information

Ordering Code	Device	Address	Package-Leads	Interface Description
TSL45311CL	TSL45311	0x39	CL-4	I^2C $V_{BUS} = V_{DD}$ Interface
TSL45313CL	TSL45313	0x39	CL-4	I^2C V_{BUS} = 1.8 V Interface
TSL45315CL	TSL45315	0x29	CL-4	I^2C $V_{BUS} = V_{DD}$ Interface
TSL45317CL	TSL45317	0x29	CL-4	I^2C V_{BUS} = 1.8 V Interface

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Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 112A (2012-Oct) to current revision 1-00 (2016-Aug-31)	Page
Content of TAOS datasheet was converted to the latest **ams** design	
Updated Figure 1	1
Updated Figure 4	3
Updated Figure 8	6
Updated Figure 9	7
Updated Figure 28	21

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide